Monolithically Integrated Sigma-Delta Frequency Synthesizers in 0.13 μm CMOS

Von der Fakultät für Mathematik, Naturwissenschaften und Informatik
der Brandenburgischen Technischen Universität Cottbus

zur Erlangung des akademischen Grades

Doktor der Ingenieurwissenschaften
(**Dr.-Ing.**)

genehmigte Dissertation

vorgelegt von

Magister

Valentyn Anatoliiovych Solomko

geboren am **09.05.1982** in **Kiew** (**Ukraine**)

Gutachter: **Prof. Dr. Heinrich Klar (TU Berlin)**

Gutachter: **Prof. Dr. Georg Böck (TU Berlin)**

Gutachter: **Prof. Dr. Peter Weger (BTU Cottbus)**

Tag der mündlichen Prüfung: **8. Juli 2008**

Acknowledgements

I would like to express sincere appreciation to my advisor Prof. Dr. Peter Weger for his support over this work.

I would like to express profound gratitude to my father Dr. A. V. Solomko for sharing his broad experience in scientific matters and his invaluable encouragement throughout this research work.

I am grateful to Denys Martynenko for his designs used in developed devices, many helpful discussions and support, Oleksiy Gerasika for valuable help throughout the study and hardware designs used in measurement setups, Andriy Vasylyev, and Wojciech Debski for their informative discussions.

I would like to acknowledge Werner Simbürger and Günther Tränkle from Infineon Technologies for support in chip fabrication, Christoph Sandner for the help in answering many questions concerning research topic.

Finally, I am especially indebted to my mother and brother for their indefatigable faith and support throughout my life.

Abstract

In this work a compact, monolithically integrated, high frequency sigma-delta phase-locked loops (PLLs) designed in 0.13 μm CMOS technology are investigated. The research focuses on the analysis of PLL spurious performance degradation caused by the integrated digital sigma-delta modulator, design and optimization of compact sigma-delta modulators with improved tonal and switching noise performance.

The main achievements of this work include:

1. An implementation of MASH (multistage) modulator in the dual edge triggered style is proposed. The implementation offers two advantages over conventional MASH when integrated into the same die with a fractional-N PLL: 1) the modulator's area is reduced by 15–20%; 2) the switching noise power is distributed in such a manner, that the first reference spur of a synthesizer is not degraded; instead, the glitch energy is shifted to the second multiple of reference frequency; in the work a benefit of such reference spur power distribution is demonstrated. Proposed implementation does not affect logical behavior of the MASH modulator.

2. MASH 1-1-1 (three stages of first order each) sigma-delta modulator with DC dithering used for frequency synthesis applications is investigated. At the expense of minimum additional hardware such dithering topology allows to shift tones to the low frequencies and decrease their power.

3. An oscillator-based dither generator is proposed for the use in MASH 1-1-1 modulator. The generator consumes less current and area, produces much less supply switching noise than a conventional pseudo-random dither generator while keeping modulator's output free of tones. An empirical study of oscillator-based dither generator is presented.

4. MASH 1-1-1 modulator with direct feedback dithering is investigated. Such dithering topology requires no additional hardware to be implemented. Among the disadvantages of the direct feedback dithering is the addition of small DC offset to the output of MASH modulator and presence of some low power tones in amplitude spectrum.

Two fully integrated 11 GHz sigma-delta PLLs incorporating single- and dual edge triggered MASH modulators with different dithering topologies were fabri-

cated in 0.13 μm CMOS process. Spurious, as well as phase noise performance of the PLLs for different modulator topologies was compared. The PLL controlled by the integrated dual edge triggered MASH 1-1-1 modulator exhibited first reference spur below –66 dBc over the whole locking range and fractional spurs power not exceeding –70 dBc within 70% of the division ratio range.

Zusammenfassung

In der vorliegenden Arbeit werden kompakte, monolithisch integrierte Hochfrequenz Sigma-Delta Phasenregelschleifen (PLLs), die in einer 0.13 μm CMOS Technologie realisiert wurden, untersucht. Die Untersuchung befasst sich mit der Analyse von harmonischen Störungen im Spektrum der PLL, die vom integrierten digitalen Sigma-Delta Modulator verursacht werden, sowie mit der Entwicklung und der Optimierung von Sigma-Delta Modulatoren mit geringen harmonischen Komponenten am Ausgang und verringerten digitalen Schaltrauschen.

Wichtige Ergebnisse dieser Arbeit sind:

1. Die Entwicklung vom doppelflankengesteuerten kaskadierten Modulator (bezeichnet als MASH Architektur), der in Sigma-Delta Frequenzsynthesizern angewendet wird. Bei einer gemeinsamen Integration vom MASH Modulator und der Fractional-N PLL, bietet diese Verwendung zwei Vorteile: 1) Die Fläche des Modulators wird bis zu 15–20% reduziert; 2) Das Schaltrauschen wird verteilt, damit die harmonische Komponente bei Abstand von einer Referenzfrequenz zum Träger nicht vergrößert wird. Die Schaltrauschenleistung bzw. unerwunschte harmonische Störungen werden auf einen doppelnen Referenzfrequenzabstand verschoben. In der vorliegenden Arbeit werden die Vorteile solcher Schaltrauschenverteilung demonstriert. Bei doppelflankengesteuerter Realisierung wird die Logikfunktion des Modulators nicht verändert.

2. MASH 1-1-1 (drei kaskadierte Modulatoren erster Ordnung) Sigma-Delta Modulator mit DC-Dither in Anwendung auf Sigma-Delta Frequenzsynthesizern wird untersucht. Eine solche Dither-Funktion wird mit weniger zusatzlichen Komponenten realisiert. Mit Hilfe des DC-Dithers wird die Frequenz der harmonischen Störungen verkleinert und ihre Leistung wird verringert.

3. Ein Oszillator-basierter Dither Generator in Anwendung auf ein MASH 1-1-1 Modulator wurde entwickelt. Einerseits verbraucht der Generator weniger Strom und Chipfläche und produziert weniger Schaltrauschen als ein üblicher digitaler Pseudozufallgenerator, andererseits unterdrückt er effektiv die harmonischen Komponenten am Ausgang des Modulators. Eine empirische Analyse des Oszillator-basierten Dither Generators wird dargestellt.

4. Ein MASH 1-1-1 Modulator mit direktem rückgekoppelten Dither wurde untersucht. Direktes rückgekoppeltes Dither wird ohne zusatzliche Komponenten realisiert. Als Nachteil dieser Methode wird ein kleiner DC-Wert zum Eingangssignal des Modulators addiert. Auch die harmonischen Störungen werden nicht völlig unterdrückt.

Zur experimentellen Verifikation wurden zwei völlintegrierte 11 GHz Sigma-Delta PLLs mit einzel- und doppelflankengesteuerten MASH Modulatoren mit verschiedenen Dither Verwertungen in einer 0.13 μm CMOS Technologie hergestellt. Sowohl harmonische Störungen als auch Phasenrauschen des Eingangssignals der PLLs wurden verglichen. Bei Benutzung des integrierten doppelflankengesteuerten MASH Modulators liegt die störende Frequenzkomponente unter –66 dBc bei einem Referenzfrequenzabstand zum Träger. Die fractional harmonischen Komponenten liegen unterhalb –70 dBc innerhalb von 70% vom eingerasteten Frequenzbereich.

Contents

List of Abbreviations

AC	**A**lternating **C**urrent
ADC	**A**nalog to **D**igital **C**onverter
BCD	**B**inary-**C**oded **D**ecimal
CML	**C**urrent **M**ode **L**ogic
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
DAC	**D**igital to **A**nalog **C**onverter
DC	**D**irect **C**urrent
DDS	**D**irect **D**igital **S**ynthesizer
DET	**D**ual **E**dge **T**riggered
FA	**F**ull **A**dder
FM	**F**requency **M**odulation
ISM	**I**ndustrial, **S**cientific and **M**edical
LO	**L**ocal **O**scillator
MASH	Multi-stage noise shaping
MIM	**M**etal-**I**nsulator-**M**etal
MOS	**M**etal **O**xide **S**emiconductor
MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
NTF	**N**oise **T**ransfer **F**unction
PCB	**P**rinted **C**ircuit **B**oard
PFD	**P**hase **F**requency **D**etector
PLL	**P**hase-**L**ocked **L**oop
PN	**P**seudo **N**oise
PPCL	**P**ush-**P**ull **C**ascode **L**ogic
PSD	**P**ower **S**pectral **D**ensity
SMD	**S**urface **M**ount **D**evice
SoC	**S**ystem-**o**n-**C**hip
SOI	**S**ilicon **O**n **I**nsulator
SET	**S**ingle **E**dge **T**riggered
SSB	**S**ingle **S**ideband
STI	**S**hallow **T**rench **I**solation
STF	**S**ignal **T**ransfer **F**unction
VCO	**V**oltage **C**ontrolled **O**scillator
VLSI	**V**ery **L**arge **S**cale **I**ntegration
XO	Crystal/Quartz **O**scillator

Chapter 1

Introduction

Motivation

The number of users of wireless communication devices has grown spectacularly over the last decade and still continues growing. This resulted from successful transition of analog radio-frequency circuits into the IC level, which allowed fabricating sophisticated, reliable, and cheap products.

Evolution of wireless communication market constantly challenges engineers to look for low-cost, low-power, and high performance solutions applied to well established, widely used standards, as well as new-coming, developing wireless technologies.

Nowadays wireless second- and third-generation short-range communication networks are materialized in the IEEE 802.11a,b,g and forthcoming IEEE 802.11n standards operating in 5 GHz and 2.4 GHz public spectrum bands. The latter could provide maximum data rate of few hundred megabits per second. However, due to the growing user demands even such data rates seem to become insufficient in the nearest future. Thus, efforts are made to develop short-range multiband systems operating in 5, 17, 24, 38, and 60 GHz ISM bands offering data rates of up to 1 Gb/s [Ebert 05].

To achieve high data rates not only increased channel bandwidth or the use of heterogeneous system concept is necessary, but also sophisticated modulation schemes are required. This, in turn, is accomplished only by the powerful digital baseband processors together with precise RF analog front-end. Finally, to be competitive on the market manufacturing cost of hardware product must be low.

Only highly integrated system-on-chip (SoC) solutions can meet such strict performance and cost requirements. CMOS and BiCMOS technologies allow integrating DSP features and RF front-end on a same semiconductor die. Much progress has been made in implementing single-chip transceivers [Zhang 05] as well as mixed RF-analog-digital systems on a chip [Eynde 01] operating in 2.4 GHz and 5 GHz bands. Efforts are made to design 17 GHz monolithically integrated

transceivers in submicron CMOS technologies [Tiebout 05]. Individual transceiver sections for 24 GHz and 60 GHz fabricated in CMOS and BiCMOS are already presented in literature [Debski 07], [Winkler 05] and the task of uniting them into a single-chip solution is forthcoming.

Frequency synthesizer is an essential part of a transceiver. Fig. 1.1 illustrates the role of a synthesizer in heterodyne transceiver. Currently phase-locked loop (PLL) based frequency synthesizers offer the best performance tradeoff among all frequency synthesis methods and are the most widely used in high frequency integrated transceivers.

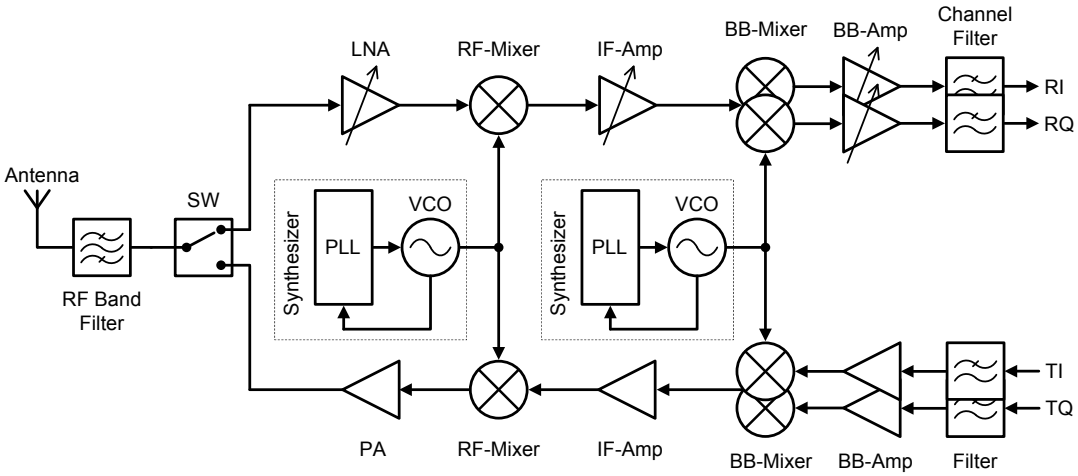


Figure 1.1: Frequency synthesizer in heterodyne I/Q transceiver

Driven by the rapid development and introduction into mass production of submicron CMOS technologies, historically popular integer-N PLLs are now being more and more often replaced by sigma-delta frequency synthesizers. The use of sigma-delta phase-locked loops in communication standards with relatively high channel bandwidth makes sense to relax the requirements to the frequency standard (quartz oscillator) used for synthesizer synchronization: fine frequency resolution allows to compensate crystal frequency drift and avoid the necessity of reference frequency which is an integer multiply of channel center frequency. Various single-chip transceiver designs employing integrated sigma-delta frequency synthesizers operating in ISM band were recently reported in literature [Tiebout 05], [Zhang 05].

Being a mixed-signal analog-digital system, sigma-delta PLL is inherently sensitive to such technologically-defined factors as the amount of substrate noise coupling, quality of active devices and passive structures. As the dimensions of chip features and supply voltage evolutionary scale down, the problems of reduced dynamic range and increased phase noise and digital noise coupling are becoming dominant [Abidi 04]. This unavoidably introduce new challenges in CMOS sigma-delta synthesizer design. Thus, the problem of developing new and optimization

of already known solutions for monolithically integrated sigma-delta frequency synthesizers designed in submicron CMOS technologies is urgent and considered in this work.

Research Goal and Objectives

The goal of research is performance improvement and cost reduction of high-frequency, monolithically integrated sigma-delta phase-locked loops fabricated in deep-submicron CMOS technologies by means of architectural, layout, and circuit-level modifications and optimization of synthesizer compound blocks. Research efforts have been put mainly on spurious performance improvement, however, other performance issues are also considered.

To achieve the posed goal the following objectives are accomplished:

1. Design of an 11 GHz PLL core in 0.13 μm CMOS technology for investigating the influence of sigma-delta modulator on the performance of frequency synthesizer; the core should employ phase-frequency detector, charge pump, loop filter, VCO, and programmable feedback frequency divider for operating in fractional-N mode.

2. Evaluate the influence of integrated sigma-delta modulator (as one of the substantial switching circuits in frequency synthesizer) on spurious performance of the system; develop and investigate architectural, layout, and circuit design solutions aimed at reducing performance degradation caused by the influence of digital noise coupling from on-chip sigma-delta modulator.

3. Investigate architectures and schematic implementations of tone-free digital sigma-delta modulators.

4. Elaborate reduced-area realization of conventional sigma-delta modulator designed in CMOS logic.

5. Develop the measurement setup for evaluating spurious/phase noise performance of the fabricated devices. This objective, in turn, is subdivided into the following steps:

    - printed-circuit boards design for connecting the chip with the measurement setup;
    - implementing the algorithms and software for programming the synthesizer and measurement equipment;
    - implementing external (off-chip) sigma-delta modulator in FPGA.

Support by Research Programs

The work was partly supported by the WIGWAM research project [Ebert 05] which is pursued in cooperation with Infineon Technologies AG and other 26 industrial and research institutions.

Extent of Research Work

All hardware for research (test structures and entire synthesizer chips) was fabricated during 7 tapeouts under Infineon 0.13 μm CMOS C11RF and C11N technologies over a period of two years. The detailed measurement results of two synthesizer chips are presented in the dissertation.

Thesis Organization

The second Chapter gives an introduction into the sigma-delta frequency synthesis techniques, states the scope of the investigation and presents a brief overview of the prior work. In Chapter 3 an insight into mixed-signal interaction aspects in the integrated synthesizers is given, the known circuit-level and layout solutions of the problem are discussed. Chapter 4 starts with the conventional implementations of sigma-delta modulators and continues with the proposed solutions. Theoretical findings as well as the simulation results are presented in this section. In Chapter 5 the implementation details of the devices for experimental verification of the proposed concepts are presented. The measurement results are given in Chapter 6. Finally, Chapter 7 concludes the dissertation.

Chapter 2

Problem Statement

2.1 Area of Focus

2.1.1 PLL Based Frequency Synthesis Techniques

Integer-N PLL

Integer-N PLL is widely used in RF transceivers for generating stable, precisely defined LO signal. Fig. 2.1 illustrates the block diagram of an integer-N PLL.

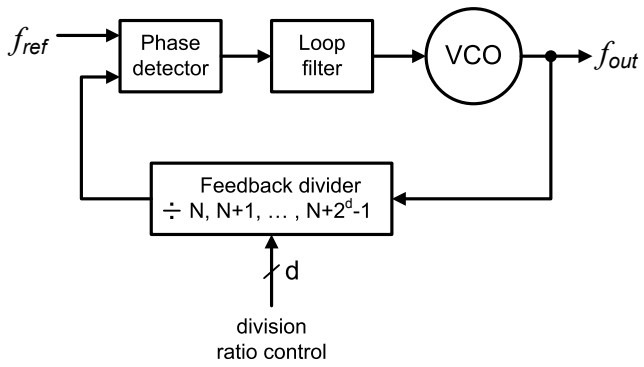


Figure 2.1: Integer-N phase-locked loop

Generated frequency defines as:

$$f_{out} = K \cdot f_{ref} \tag{2.1}$$

where f_{ref} is a reference frequency, $K \in \{N, \ldots, N + 2^d - 1\}$ – frequency division ratio.

Triggered by the VCO output signal (which defines the fundamental quantization step-size in the system), divider can provide only integer values of K. This immediately reveals the limitations of integer-N architecture:

- Channel center frequency/intermediate frequency must be an integer multiply of reference frequency;
- Channel spacing must be an integer multiply of reference frequency.

Such property of an integer-N PLL to tie the output frequency with the reference frequency applies strong restrictions on the crystal oscillators used as a frequency standard. The choice of a single reference becomes even more complicated (if possible) if transceiver is intended to operate in multiple bands or multiple communication standards. Moreover, unavoidable frequency drift of a crystal oscillators caused by ageing cannot be compensated in conventional integer-N architecture resulting in overall transceiver performance degradation.

Fractional-N PLL

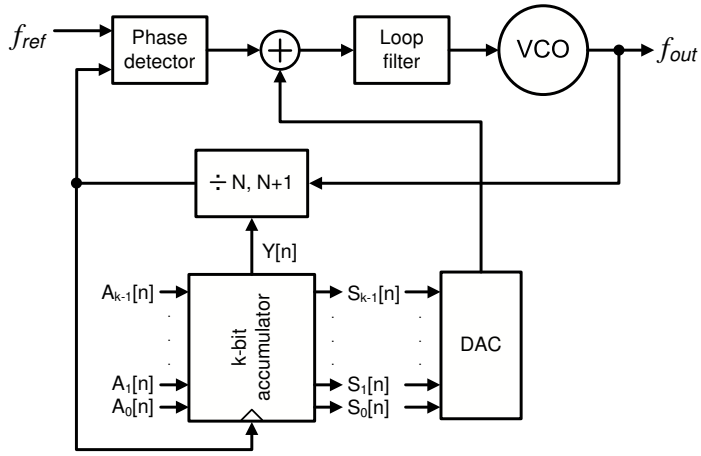
Fractional-N architecture eliminates the restrictions of an integer-N PLL. It allows the LO frequency and frequency step to be a fractional multiply of reference frequency. The result is achieved at the expense of additional digital (and in some modifications analog) hardware. Frequency resolution is defined only by a digital control circuitry and can be relatively high.

Synchronized by an arbitrary quartz oscillator fractional-N phase-locked loop can easily lock VCO at any frequency within its tuning range. Reference frequency drift caused by ageing and temperature change can also be easily compensated, relaxing the requirements to precision of reference oscillator.

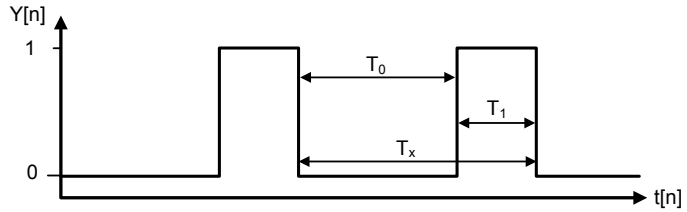
Fractional-N technique implemented in sigma-delta frequency synthesizers is constantly gaining popularity and becoming more widely used in integrated, especial multi-band, multi-standard commercial transceivers [SMA06].

2.1.2 Accumulator-Based Fractional-N PLL

Fractional-N division technique was first realized in digiphase synthesizer [Gillette 69]. Integer as well as fractional division of VCO signal was performed by means of a BCD accumulator. Most significant digits of accumulator's control word were responsible for integer division, while least significant digits serve for precise output frequency definition. Moreover, digital-to-analog converter driven by the fractional cycle residue was used for compensating periodic modulation of the VCO carrier and suppressing severe spurious tones at the output. Fig. 2.2 illustrates an accumulator-based fractional-N PLL (which differs from the digiphase synthesizer but saves the main principle of operation).



(a)



(b)

Figure 2.2: (a) – fractional-N PLL controlled by accumulator with DAC compensation, (b) – waveform observed at the overflow terminal of accumulator

State space representation of k-bit digital accumulator is described by (2.2) and (2.3):

$$S[n+1] = \begin{cases} S[n] + A[n+1], & \text{if } S[n] + A[n+1] < 1; \\ S[n] + A[n+1] - 1, & \text{if } S[n] + A[n+1] \geq 1. \end{cases} \tag{2.2}$$

$$Y[n+1] = \begin{cases} 0, & \text{if } S[n] + A[n+1] < 1; \\ 1, & \text{if } S[n] + A[n+1] \geq 1, \end{cases} \tag{2.3}$$

where $A[n] = (A_0[n] + A_1[n] \cdot 2 + \ldots + A_{k-1}[n] \cdot 2^{k-1})/2^k$, $S[n] = (S_0[n] + S_1[n] \cdot 2 + \ldots + S_{k-1}[n] \cdot 2^{k-1})/2^k$, and $A_i[n] \in \{0; 1\}$ – i-th bit of the input signal.

Note that $A[n]$ is a fractional number, which falls in the range $0 \leq A[n] < 1$. Though it is common to represent a digital number by corresponding integer, in the case of input control words for digital sigma-delta modulators used in fractional-N PLL its more convenient to represent $A[n]$ as a rational number which equals the fractional part of a division ratio.

When overflow occurs (i.e. $Y[n] = 1$), division ratio is set to $N + 1$, otherwise division ratio equals N. Obviously, the higher the value of accumulator's input

signal, the more often overflow is generated. Fig. 2.2(b) shows an example of the waveform of overflow signal. Referring to this waveform, an average division ratio over some period T_x can be calculated:

$$N_A = \frac{T_0 N + T_1(N+1)}{T_0 + T_1} \tag{2.4}$$

where T_0 is a part of time period when division by N is performed, T_1 is a part of time period when division by $N+1$ is performed.

If constant control signal $A[n] = const$ is applied to the accumulator, then N_A can be expressed through the $A[n]$ [Kingsford-Sm 75]:

$$N_A = N + A[n] \tag{2.5}$$

Finally, PLL output frequency defined as

$$f_{out} = N_A \cdot f_{ref} = (N + A[n]) \cdot f_{ref}, \tag{2.6}$$

is a rational multiply of reference frequency. Output frequency range is limited by the divider ($N_A \cdot f_{ref} \leq f_{out} \leq (N_A + 1) \cdot f_{ref}$), whereas resolution is defined by the capacity of accumulator – frequency step can not exceed $\Delta f_{out} = f_{ref}/2^k$.

With the help of DAC cancellation technique fractional spurs power of –70 dBc can be achieved [Miller 91]. Better spurious suppression in such architecture is problematic because of mismatches between DAC and PFD.

2.1.3 Sigma-Delta PLL

Generic Sigma-Delta Fractional-N Phase-Locked Loop

To improve spectral purity achieved by the prior art, the use of high order sigma-delta modulators for controlling frequency divider was proposed [Miller 91]. In spite of the fact that accumulator used in the first fractional PLL is also a first order digital sigma-delta modulator, according to definition adopted de facto in literature, sigma-delta PLL is used to comprise a modulator with an order of two or higher. A block diagram of a sigma-delta PLL is pictured in Fig. 2.3. Such architecture significantly improves the bottleneck of conventional accumulator-based PLL – poor fractional spurious performance.

The output frequency of the synthesizer is defined as

$$f_{out} = N_A \cdot f_{ref}, \tag{2.7}$$

where N_A is the average division ratio of the divider.

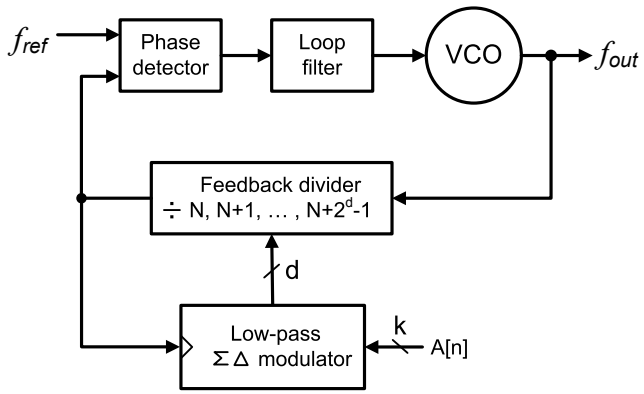


Figure 2.3: Sigma-delta PLL block diagram

Digital sigma-delta modulator performs a role of a control circuit for divider and provides the desired average division ratio. Controlling the divider with a small number of integer division ratios 2^d by means of sigma-delta modulator, a large number of fractional division ratios 2^k can be obtained. In other words, sigma-delta modulator concentrates the input digital DC signal with high resolution into the output digital AC signal with low resolution which corresponds to the input one. The following conditions hold true:

$$d < k, 2^d \ll 2^k \tag{2.8}$$

where d is a number of bits in control word of the divider, and k is a number of input bits of the sigma-delta modulator.

In the same fashion as sigma-delta ADC approximates continues amplitude analog signal by the discrete amplitude signal, digital sigma-delta modulator represents high resolution digital signal by another low resolution digital signal, see Fig. 2.4. Moreover, unlike in Nyquist converters, feedback quantizers feature frequency dependent quantization error. Specifically, low-pass sigma-delta modulators used in PLL exhibit zero quantization error for static input signals, meaning that average value of the converted signal *exactly* matches the input DC signal applied to the modulator. Both analog and digital modulators could perform a role of a control circuit for the frequency divider, but digital sigma-delta modulators are preferable since average division ratio is exactly defined by the digital control signal.

Sigma-delta modulator's architecture has an essential influence on the PLL performance and always entails a tradeoff between spurious and phase noise power. By decreasing the closed loop PLL bandwidths to the values below 100 kHz a good spurious–phase noise compromise can be met [Meninger 05]. This, however, diminishes some advantages of fractional-N synthesis technique. In spite of the drawbacks sigma-delta phase-locked loop becomes more frequently used architecture for RF applications at the moment.

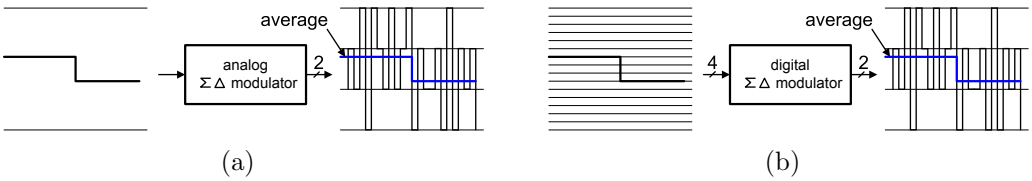


Figure 2.4: Analog versus digital sigma-delta modulator

Alternative Implementations of Sigma-Delta PLL

A technique analogous to DAC compensation in accumulator-based fractional PLL was applied to sigma-delta PLL [Temporiti 04], [Meninger 05]. DAC-compensated PLL, illustrated in Fig. 2.5, having the bandwidth of about 1 MHz, demonstrates good suppression of the sigma-delta modulator's quantization noise at high offset frequencies. The bottleneck of the architecture is a precise matching between phase error and DAC compensation signal.

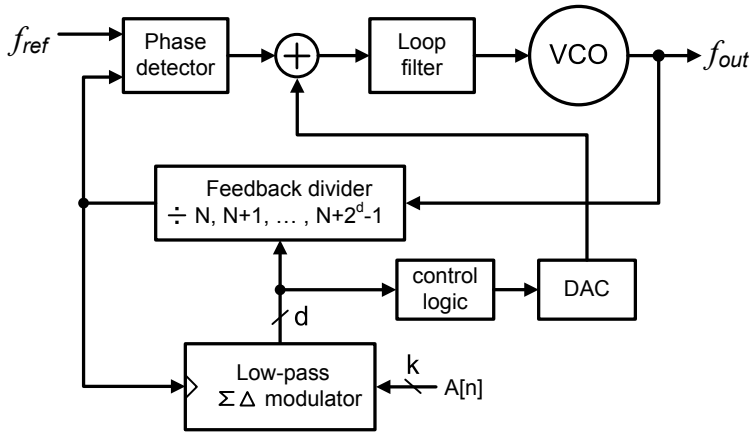


Figure 2.5: Sigma-delta PLL with DAC compensation

An alternative approach for improving spectral purity degradation caused by sigma-delta quantization is to break the period of the VCO signal into smaller parts (i.e. generate several signals which have the same period but different phases) and then use these parts for performing fractional division [Park 01]. The amplitude of the phase error will be decreased and phase noise/spurious performance improved. Multiphase technique makes sense only with ring oscillators. With LC-VCOs, especially those which operate at high frequencies, the minimum triggering time step defines by the carrier period and practically cannot be divided by smaller fractions.

In Fig. 2.6 an alternative to generic fractional-N synthesizer is shown. Here reference frequency divider controlled by sigma-delta modulator is used. In such architecture the output frequency of the synthesizer is expressed as follows:

$$f_{out} = \frac{N}{N_{R.A}} \cdot f_{ref}, \tag{2.9}$$

where $N_{R.A}$ is the average division ratio of a reference divider.

Such architecture, however, is seldom used in practical devices because of the higher noise contribution of sigma-delta modulator.

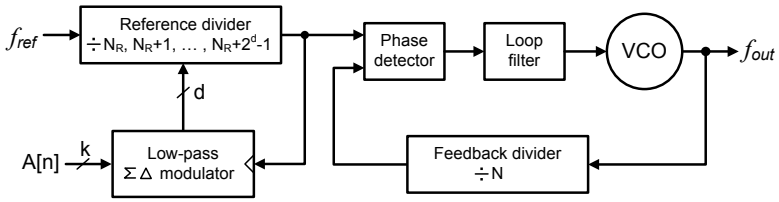


Figure 2.6: Sigma-delta PLL comprising reference frequency divider

In [Hernandez 96] the use of bandpass sigma-delta modulator as a reference source is proposed, see Fig. 2.7. The idea is to use low-frequency direct digital synthesizer (DDS) based on band-pass sigma-delta modulator for generating reference frequency. The whole synthesizer is realized at the expense of additional digital and analog hardware and several times higher reference frequency than required for architecture shown in Fig. 2.3.

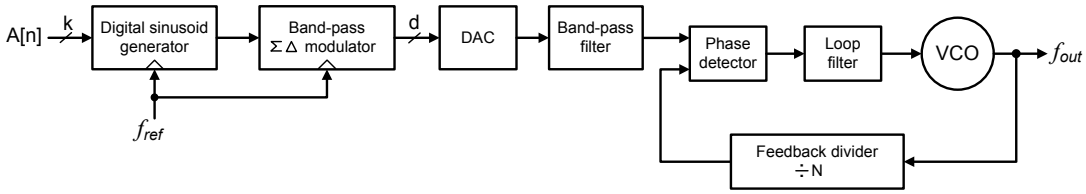


Figure 2.7: Block diagram of the fractional-N PLL based on a band-pass sigma-delta modulator

One can introduce modulation information into the loop by means of sigma-delta modulator [Perrott 97]. Even if the information bandwidth is much higher than the bandwidth of the PLL, digital compensation filtering can help to modulate a carrier without the loss of information.

2.1.4 Area of Focus

In this work only the heterodyne transceiver architecture where a PLL performs a role of high frequency carrier generator for up- or downconversion mixers is considered. It follows, that digital sigma-delta modulators operating only with

static input signals are investigated. Sigma-delta PLL with feedback low-pass modulator without DAC compensation is considered.

Finally, based on the tasks of research and most efficient solutions available at the moment, only the following sigma-delta modulators will be considered further in this work:

1. Fully digital modulators comprising digital input and generating digital output;
2. Low-pass sigma-delta modulators controlling feedback frequency divider;
3. Operating conditions: only static (DC) digital signal is applied to the input of the modulator.

2.2 Scope of Investigation

Fractional-N synthesizers in general and sigma-delta synthesizers in particular are known to suffer from spurious tones or sidebands. In integrated synthesizers this parasitic effect is even more pronounced because of the noise coupling within the shared die and even radiation from the wires/bondwires into the sensitive analog blocks. Sidebands degrade the spectral purity of the generated signal.

Sidebands in sigma-delta synthesizers are subdivided into fractional and reference spurs. The diagram in Fig. 2.8 categorizes the spurious tones in integrated sigma-delta PLLs and shows their origins.

Fractional spurs are caused mainly by two factors: tonal behavior of digital sigma-delta modulator and phase error distortion due to nonlinearities in the analog blocks of the loop. By using dithered, high order, multibit modulator, which is able to generate highly decorrelated digital sequence, tones in sigma-delta modulator can be efficiently suppressed [Norsworthy 97]. Nonlinear distortions are introduced principally during $\Delta\varphi \rightarrow I_{CP}$ conversion, namely, by dead-zones in phase-frequency detector and current mismatches in charge pump [Muer 02].

Recently a new mechanism that is possibly responsible for the production of fractional spurious components was reported in literature [Brennan 04]. According to [Brennan 04] fractional spurs are caused by intermodulation and aliasing resulting from the phase detector nonlinear action with the presence of two non-harmonically related frequency components in fractional-N PLL: reference frequency and VCO frequency. In [Brennan 04] basic theoretical analysis of intermodulation effect is given. At present this effect is not considered dominant or even significant in fractional spur generation. However, as the degree of integration evolutionary goes up the intermodulation mechanism can gain more influence on fractional spurs generation in future integrated synthesizers fabricated in CMOS technologies with smaller feature size.

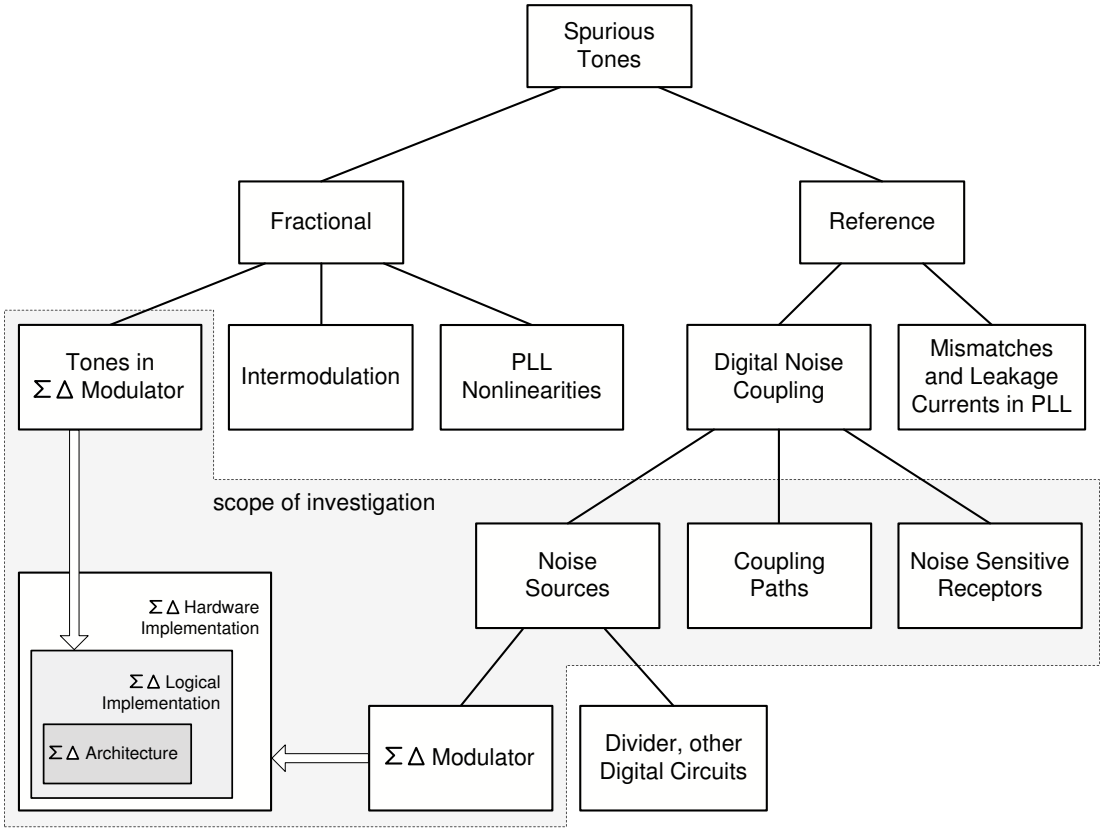


Figure 2.8: Spurious tones in monolithically integrated sigma-delta PLLs

Reference spurs are the result of mismatched charge pump, leakage currents in the loop filter, or a digital noise coupling into the sensitive analog components of the loop. In compact, monolithically integrated sigma-delta PLL reference spurs caused by digital noise coupling can easily exceed fractional spurs level.

Expanding digital noise coupling effects three basic mechanisms should be considered: noise sources, coupling paths, and noise sensitive receptors. Sigma-delta modulator, frequency divider, digital input/output buffers implemented in CMOS logic belong to the digital noise sources in the integrated mixed-signal system. The latter, however, are often implemented in low-noise differential CML logic and disabled if not required for system operation.

Though from the first glance it may seem that fractional sidebands caused by idle tones in sigma-delta modulator, and reference spurs due to the digital noise coupling are not related each to the other, closer look reveals that common origins can still be found. Consider an implementation of integrated digital sigma-delta modulator in the way it is shown in Fig. 2.8. It contains three levels: architectural, logical, and hardware. Sigma-delta architecture occupies the highest hierarchical level and defines general structure of the device. Linear model in z-domain presents the architecture of sigma-delta modulator. Logical implementation de-

fines the resolution of device and assembly of each block with primitive gates and registers. Having the logical implementation, a tonal behavior of the modulator can be predicted. Hardware implementation based on both architectural and logical levels finally defines the structure of sigma-delta modulator. Here, under hardware implementation, circuit and layout realization is meant. Hardware implementation has no influence on the tonal performance of sigma-delta modulator since it only materializes the finite state machine logic, but does not modify it. However, when treated as a switching noise source, hardware implementation (which, in turn, is strongly influenced by the logical model) must be considered.

Every specific modulator's function can be implemented in hardware in various ways. Depending on the implementation switching noise properties will also be different. For example, either CMOS or differential current-mode logic (CML) styles can be used to implement basic logic functions. CML logic is known to demonstrate superior digital noise performance over the CMOS implementation. However, higher current consumption and occupied area, lower robustness (CML logic appears to need interstage level matching) made it rarely used in low-cost, portable integrated designs. If registers are implemented in CMOS dual-edge triggered style, switching events will be distributed in time which alter the noise induced onto the sensitive receptors.

Another approach is to change the modulator's architecture and/or logic in such a manner that its hardware realization becomes noise superior. For instance, in [Yang 06] the resolution of each stage of MASH 1-1-1 modulator is not the same as in conventional structure, but each following stage is truncated to the lower bit count. As claimed in the paper, performance of the reduced modulator is not degraded, yet chip area, power consumption and very probably switching noise (the latter is not stated in the article) is reduced by 33%.

The current work focuses mainly on the investigation of architectural and circuit-level solutions of digital sigma-delta modulators aimed at improving spurious performance of the integrated sigma-delta frequency synthesizers. Special efforts are put into investigation of modulator architectures featuring tone-free output sequence on one hand, and noise superior hardware implementation on the other. Modified hardware realizations of conventional architectures offering advantageous switching noise distribution are investigated.

2.3 Prior Work

The majority of the prior work focuses on investigation of substrate noise influence on the PLL performance in general [Larsson 01], [Jenkins 06], [Heydari 04], but very little sources analyze the impact of exactly sigma-delta modulator's switching noise on the spectral purity of the PLL signal. Efforts were made to implement reduced hardware sigma-delta modulators able to offer the same performance as conventional realizations. In some works low-noise logic for hardware

implementation was used.

In [Bornoosh 05] reduced complexity 1-bit high-order digital sigma-delta modulator for low-voltage fractional-N frequency synthesis applications is proposed. Modifications are done on architectural level. Its a two-stage modulator without linear network. The first stage is 1-st order 20-bit input 8-bit output modulator. Reduced resolution bitstream is then applied to the 1-bit output 3-rd order stage. To achieve the same 'dynamic range–tones suppression–quantization noise distribution' tradeoff, reduced-complexity modulator requires 2 times less full adders and D-flip-flops than conventional implementation.

Another hardware efficient MASH 1-1-1 modulator is presented in [Ye 07]. In contrast to the conventional implementation, the device comprises first-order stages with different resolution. The highest bit-count has the first stage and the lowest bit-count has the third stage. The total gate count in realized 20-bit input MASH modulator cited in [Ye 07] is 68% of the conventional 20-bit MASH. A practical verification of hardware efficient MASH 1-1-1 modulator is given in [Yang 06], where it was implemented in the integrated fractional-N frequency synthesizer.

Another work focuses on the alternative implementation of dither generator, namely feedback dithering [Liu 05]. Here, 3-bit output sequence of MASH 1-1-1 modulator is applied to the 3-bit input accumulator and overflow bit of the accumulator goes to the carry-in terminal of the second stage of MASH 1-1-1 modulator. In some cases such architecture can offer lower gate count than the conventional MASH with pseudo-random bit generator used for dithering.

All the design solutions presented above deal with modulator's architecture or logical modifications, but do not consider transistor-level realizations.

Talking about hardware efficient modulators, spurious performance of the modern integrated sigma-delta PLL designs employing different suppression methods should be analyzed. Not so many practical implementations of fully integrated sigma-delta PLLs operating at frequencies over 10 GHz are reported in literature. The state-of-art designs at 5 GHz demonstrate reference spurious performance from –55 dBc to –60 dBc [Chen 06]. 20 GHz sigma-delta PLL cited in [Ding 07] exhibits reference spurs of –50 dBc. Fractional spurs power usually lies close to the reference spur power and ofter does not exceed the latter. 13 GHz PLL reported in [Tiebout 04] demonstrated fractional spurs of –50 dBc (however, measurements were performed at frequency four times lower than the VCO carrier). The state-of-art fractional spurs level for 2.4 GHz design is reported in [Marletta 05], where they are 63 dB below the carrier.

Chapter 3

Noise Coupling in the Integrated Synthesizers

Among one of the major performance limitation factors typical for fully integrated mixed-mode systems is a digital supply noise coupling through the common substrate. Monolithic sigma-delta phase-locked loops require to combine considerable amount of purely digital, constantly switching circuitry (like prescaler and sigma-delta modulator) together with a very sensitive analog blocks (voltage-controlled oscillator, charge pump and loop filter). Voltage drops at the ground buses caused by the current spikes generated by the switching transients in CMOS logic are transferred to the analog part of a PLL by means of a shared substrate. In improperly designed system power supply noise coupling can totally degrade its performance.

Fig. 3.1 demonstrates how the sigma-delta modulator's switching noise can degrade the spectral purity of the output signal of a PLL. Perturbations on the supply and ground buses are coupled onto the analog components of the PLL through the variety of different paths. Sigma-delta modulator is a triggered system. The supply voltage perturbations are changing with the rate of reference frequency which means that the amplitude spectrum of modulator's supply noise has a severe peaks at f_{ref}, $2f_{ref}$ and so on. Later on, these peaks appear as the spurious tones at offsets of integer multiple of reference frequency. The power of each spur depends on the frequency and amplitude of corresponding harmonic in amplitude spectrum of modulator's switching noise.

Not only the switching noise generated by CMOS logic can couple onto analog subcircuits, but also high frequency analog signals spreading over the substrate can be combined with digital signals introducing undesired jitter. If combined analog-digital signal is applied to the nonlinear or sampling circuit intermodulation can occur [Brennan 04].

Analyzing digital noise coupling effects in an integrated circuit, three factors must be taken into account:

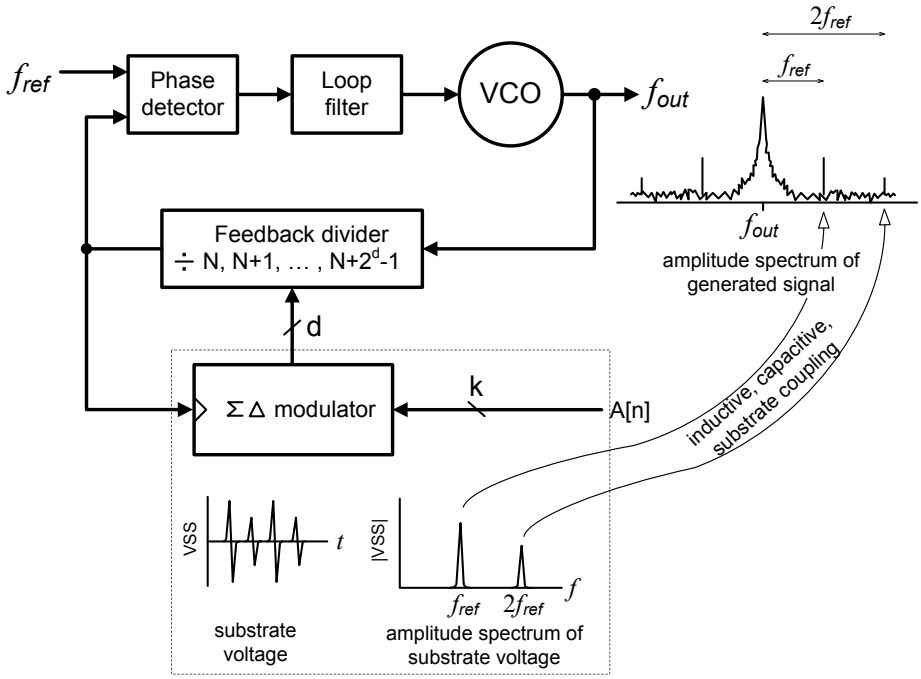


Figure 3.1: Supply noise harmonics to spurious tones mapping in an integrated sigma-delta PLL

- noise sources;
- noise sensitive receptors;
- coupling paths.

The major noise sources in the integrated sigma-delta synthesizers are frequency divider and sigma-delta modulator implemented in CMOS logic. By reducing their switching activity the amount of generated digital noise can be reduced. This is achieved by means of using low-noise logic or distribution of switching events over the time. In some cases high frequency integrated oscillator can be considered as a noise source. However, noise coming from the logic has considerably stronger influence on synthesizer's signal purity.

Integrated loop filter, VCO, phase-frequency detector and charge pump belong to the noise sensitive receptors. Differential implementation of each of these blocks makes them much more immune to the noise coupled from the digital circuitry.

Noise coupling paths are usually very hard to be accurately predicted due to different variety of mechanisms of noise transfer and distributed nature of coupling paths.

In general, several mechanism of undesired signal (noise) transfer from one part of the chip to the other were reported in literature [Roermund 04]:

1. Near-field coupling between interconnection lines. The wavelength of modern RF ICs becomes comparable with the length of connection buses inside the chip, which makes interconnections acting like antennas causing radiated emission problems in a monolithic IC. Even metal stripes as short as 1/20 of the wavelength can radiate or receive unwanted high frequency signals. For modern submicron technologies unwanted field coupling can occur if the circuit operates at frequencies higher than 10 GHz with a perturbation-sensitive parts having wires longer than 600 μm.

   Since this type of undesired coupling plays significant role only at high frequencies and its influence is several orders lower than other coupling mechanisms, it will not be considered in details further in this work.

2. Capacitive and inductive coupling through interconnection lines and bond wires.

3. Switching noise coupling through the common substrate.

The following subsections give an insight into the different mechanisms of undesired noise transfer.

3.1 Direct Capacitive Coupling Between Interconnection Lines and Substrate

The significance of noise injection effect due to the capacitive coupling increases as the IC geometry scales down. The reason of such considerable increase in capacitive cross-talk is a disproportional change of lateral and vertical dimensions of chip features – while the former are rapidly scaled down to gain cost and performance, the later remain without significant change. Reduction of lithographic image size by the factor of 2 results in a doubling of parasitic capacitance between the wires of the same metallization layer in the case when the circuit is layed out according to the minimum design rules [Gal 95].

Fig. 3.2 illustrates the main parasitic capacitive elements between a chip substrate and two lowermost metallization layers. Interwiring capacitances (C_{M1}, C_{M1M2}) and metallization versus substrate capacitances (C_{M1S}, C_{M2S}) provide a path for noise injection into the sensitive nodes. A sense node can belong either to analog block (bandgap reference, VCO tuning node) or to the switching circuit, for instance, phase-frequency detector.

In order to illustrate the significance of unwanted capacitive coupling influence on the PLL spurious performance the following example is given. Consider a clock bus crossing a wire of adjacent metallization layer which connects loop filter output with a tuning terminal of the VCO. Parasitic capacitance generated as a consequence of wire crossing equals 0.05 fF (this value is very close to the

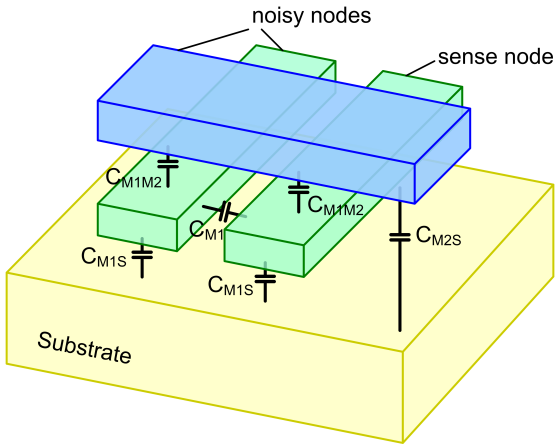


Figure 3.2: Wiring capacitive environment for noise coupling in a VLSI circuit

reality for modern submicron technologies). The clock signal is switching with a reference frequency. A circuit model for this example, consisting of a loop filter, VCO, parasitic capacitance C_p and a square-wave voltage source E_{ref}, modeling the clock transient, is shown in Fig. 3.3. Since every signal added to the VCO input is shaped by the high-pass transfer function before appearing at the output, and since reference frequency is usually one or two orders higher than the PLL bandwidth, the influence of a feedback loop is not taken into account in the model. Components values are taken from the PLL linear model described in Section 5.2.

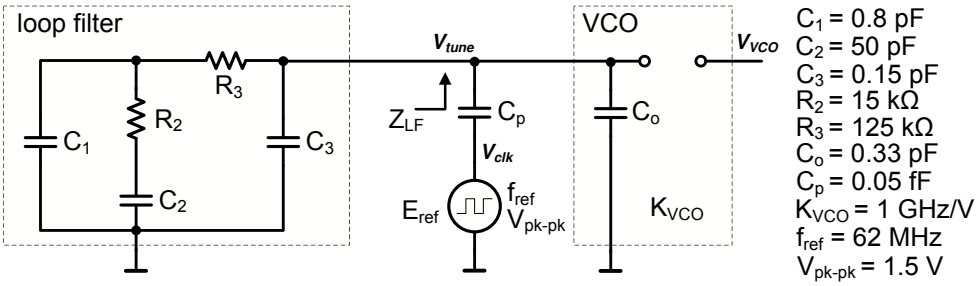


Figure 3.3: Reference spurious injection through the capacitive coupling

Clock is assumed to be a square wave signal with a peak-to-peak voltage swing of $V_{pk-pk} = 1.5\ V$. Presenting a square wave signal with a Fourier series:

$$V_{clk}(t) = \frac{2V_{pk-pk}}{\pi} \sum_{n=1}^{\infty} \frac{\sin\left((2n-1)2\pi f_{ref} t\right)}{2n-1} \tag{3.1}$$

Taking into account only fundamental harmonic, (3.1) simplifies to

$$V_{clk}(t) \approx \frac{2V_{pk-pk}}{\pi} \sin(2\pi f_{ref} t) \tag{3.2}$$

The impedance seen at the output node of a loop filter equals:

$$Z_{LF}(s) = \frac{s^2 R_2 R_3 C_1 C_2 + s(R_2 C_2 + R_3 C_2 + R_3 C_1) + 1}{s^3 R_2 R_3 C_1 C_2 C_{3o} + s^2(C_2 C_{3o}(R_2 + R_3) + C_1(R_3 C_{3o} + R_2 C_2)) + s(C_1 + C_2 + C_{3o})} \tag{3.3}$$

where $C_{3o} = C_3 + C_o$.

Substitution of components nominals into (3.3) gives the numerical value of Z_{LF} at reference frequency:

$$Z_{LF}(s)\big|_{\substack{s=j\omega \\ \omega=2\pi f_{ref}}} \approx 226 - j5333\ \Omega \tag{3.4}$$

VCO tuning voltage defines as

$$V_{tune}(s) = V_{clk}(s) \frac{Z_{LF}(s)}{Z_{LF}(s) + \frac{1}{sC_p}}, \tag{3.5}$$

where $V_{clk}(s)$ is a Laplace transform of (3.2).

Transforming (3.5) back to the time domain, considering only component at reference frequency and ignoring initial phase shift, V_{tune} expresses as

$$V_{tune}(t) = V_n \cos(2\pi f_{ref} t), \tag{3.6}$$

where V_n equals

$$V_n = |V_{tune}(s)|_{\substack{s=j\omega \\ \omega=2\pi f_{ref}}} = |0.099 + j0.0042|\, mV \approx 0.1mV \tag{3.7}$$

Frequency modulated VCO carrier in time domain defines as:

$$V_{VCO}(t) = V_A \cos(2\pi f_{VCO} t + 2\pi K_{VCO} \int_{T=0}^{t} V_{tune}(T) dT), \tag{3.8}$$

where V_A – amplitude of the output signal, f_{VCO} – VCO center frequency.

Substituting (3.6) into (3.8) gives

$$V_{VCO}(t) = V_A \cos(2\pi f_{VCO} t + \frac{V_n K_{VCO}}{f_{ref}} \sin(2\pi f_{ref} t)) \tag{3.9}$$

Since frequency modulation index $m_f = \frac{V_n K_{VCO}}{f_{ref}} = 0.0016 \ll 1$ fulfills the narrow band FM conditions, (3.9) can be approximated as [Young 94]:

$$V_{VCO}(t) \approx V_A \cos(2\pi f_{VCO} t) - \frac{V_A V_n K_{VCO}}{2 f_{ref}} (\cos(2\pi (f_{VCO} - f_{ref})t) - \cos(2\pi (f_{VCO} + f_{ref})t)) \tag{3.10}$$

Finally, relative reference spurious power, defined as a magnitude of undesired frequency component ($V_{ref} = \frac{V_A V_n K_{VCO}}{2 f_{ref}}$) divided by magnitude of the carrier (V_A), numerically equals:

$$P_{ref} = 20 \log \frac{V_n K_{VCO}}{2 f_{ref}} = -61.8 dBc \tag{3.11}$$

Decrease of the coupled voltage or VCO gain by the factor of 2 reduces the power of reference spurs by 6 dB. The same result is obtained by doubling the reference frequency. However, quartz oscillator nature limits the frequency of reference source and low K_{VCO} results in a reduced tuning range or increased settling time. Any capacitive coupling between sensitive analog parts and digital aggressors should be avoided or minimized. Very efficient practical method for minimizing an effect of capacitive noise injection is providing differential signal path for all clock and analog nodes.

3.2 Digital Noise Injection Caused by Inductive Effects

On-chip parasitic inductances formed by interconnection wires are usually not treated as a principal mechanism for digital noise coupling. For high impedance circuit nodes effect of capacitive coupling is several orders higher than that, caused by inductive influence [Roermund 04].

The most harmful are voltage bounces at low impedance supply nodes caused by current transients generated at digital supply bus. The nature of this type of noise (also known as di/dt noise) illustrates the model of a bonded chip with shared supply buses (Fig. 3.4).

Bond wire lumped element model consists of series inductance L_B and resistance R_B. Both values are frequency dependent, however as a rough approximation such dependence can be neglected. A first order formula for bond wire inductance estimation at close to DC frequencies is given in [Greenhouse 74]:

$$L_B \equiv 0.2l(\ln(2l/r) - 0.75 + r/l), \tag{3.12}$$

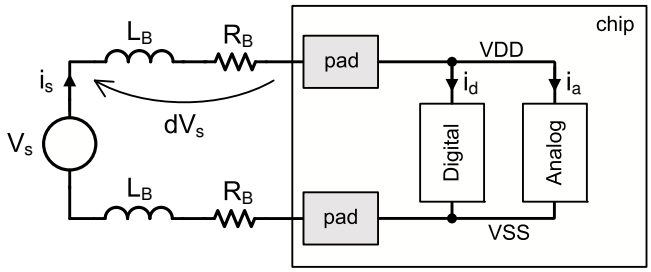


Figure 3.4: Simplified model of a bonded chip with shared supply buses

where L_B is the inductance in nH, l – conductor length in mm, r – radius of the cross section in mm. According to (3.12) 1 mm long bond wire with a radius of 12.5 μm has an inductance of 0.87 nH.

Returning to the model in Fig. 3.4, a voltage drop on the bond wire

$$dV_s = i_s R_B + L_B \frac{di_s}{dt} = (i_d + i_a)R_B + L_B \frac{d(i_d + i_a)}{dt} \tag{3.13}$$

Considering only alternating term of the voltage drop, a dominant part of dV_s is introduced by the inductive component driven by the spiky supply current of the digital blocks $L_B \cdot di_d/dt$. Since all real analog subcircuits have finite power supply rejection ratio, periodical changes in dV_s will result in spurious performance degradation of a fully integrated frequency synthesizer.

Equation (3.13) gives an insight into methods of improving supply noise performance [Larsson 99].

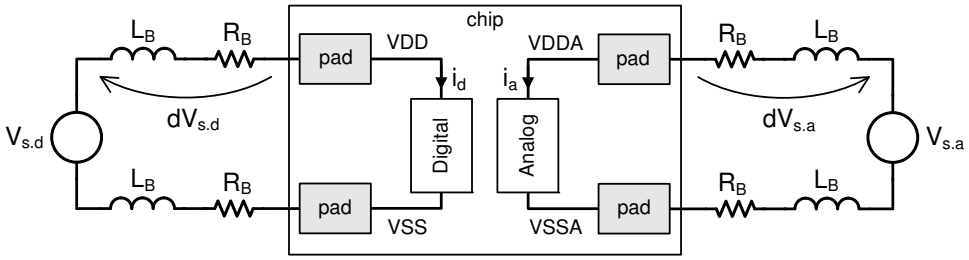


Figure 3.5: Bonded chip with separated analog and digital supply networks

1. Power supply network separation is an effective and widespread way of reducing di/dt noise influence. Fig. 3.5 demonstrates the idea. Supply voltage perturbations at digital and analog supply paths ($dV_{s.d}$ and $dV_{s.a}$) become independent on each other and noise generated at VDD and VSS nodes does not couple into analog environment (however, shared substrate still remains a path for switching noise coupling; this will be discussed in

Section 3.3). With supply network separation pad count increase. As an alternative, VDD nodes can be kept separated, while ground node may share common pad interface. A part of switching noise power can be transferred from digital to analog bondwires via magnetic coupling (not shown in the figure). Thus, it is beneficial to orient digital and analog supply bondwires at 90° to reduce noise injection through parasitic magnetic coupling [Maxim 07].

2. Decreased bond wire inductance L_B reduces the level of voltage perturbation at supply buses. This can be achieved by minimizing the length of the wire (see equation (3.12)) or by placing several bond wires in parallel. Unfortunately, the total inductance value nonlinearly depends on the number of wires places in parallel [Vasylyev 06]. Such behavior results from the relatively high mutual inductance between the adjacent bond wires. However, mutual coupling serves as a benefit when placing VSS and VDD pins in the neighborhood – the opposite direction of the current spikes at supply and ground wires causes mutual inductance subtract from the self inductance.

3. Another design consideration for minimizing digital supply noise influence is choosing low-noise logic families for implementing digital blocks, circuit optimization aimed on reducing the amplitude of current spikes at power buses generated by the logic. Obviously, combination of several techniques gives better result.

3.3 Switching Noise Injection Through the Common Substrate

Nonzero substrate conductance creates a path for digital noise distribution over the shared die. In complete monolithic mixed-signal systems utilizing both sensitive analog and switching digital parts substrate noise coupling can become a limiting factor for maximum achievable performance.

The problem of di/dt noise distribution in the integrated circuits has been extensively studied and experimental results, as well as mathematical models, were widely reported in literature. Nevertheless, prediction of performance degradation caused by the substrate noise coupling in the VLSI circuits still remains very resource and time consuming task because of the distributed nature of the noise path. For precise simulation an information about the final circuit layout is required and in the case of unsatisfied system performance due to the noise effect influence full redesign procedure is required. Very often the task of substrate noise coupling minimization in complex mixed-signal ICs requires trial-and-error solution. That's why understanding of switching noise distribution mechanisms for preventing mistakes at the first design iteration is of top importance in fully integrated frequency synthesizer design.

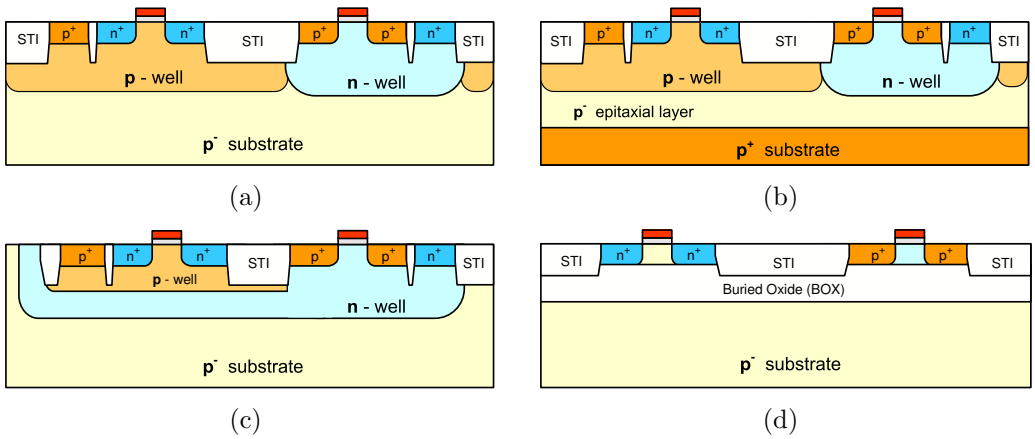


Figure 3.6: Substrate types in CMOS technology (a) – lightly doped (high resistive) substrate, (b) – epitaxial substrate, (c) – tripple-well CMOS substrate, (d) – CMOS SOI substrate

Digital noise performance of the monolithic integrated IC strongly depends on the substrate used in fabrication technology and specific technological steps aimed at improving noise coupling immunity. Fig. 3.6 illustrates four substrate types commonly used in CMOS processes. As a standard CMOS technologies twin well (or sometimes called twin-tub) technologies are considered since such kind of substrate was used for device fabrication presented in this work.

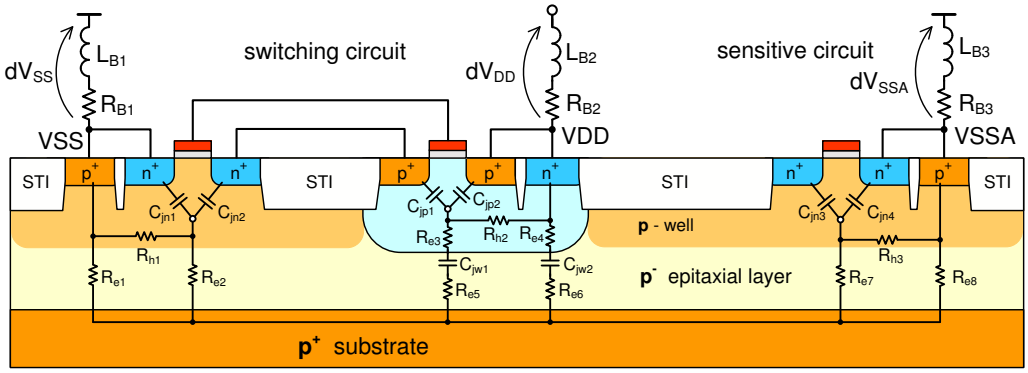
Epitaxial substrate embodies heavily doped thick p^+-type silicon bulk on a top of which lightly doped thin epitaxial layer is grown. The epitaxial layer has a thickness of 4–7 μm and a resistivity of ρ = 10–20 Ω-cm, while the bulk layer is much thicker (150–400 μm) and its resistivity commonly ranges from 0.01 Ω-cm to 0.05 Ω-cm. The resistivity of p- and n-wells is usually one order lower than in epitaxial layer. The thickness of wells is several micrometers. Field implant under the STI usually is grown for preventing parasitic channel appearance below isolation and decreasing leakage current between neighboring transistors [Johns 97]. High latch-up immunity made epitaxial substrate popular for processing CMOS circuits [Backenius 07]. However, the presence of thick low resistive silicon layer makes epitaxial substrate not the best choice when the minimum digital noise coupling is required.

Much better switching noise performance demonstrates high resistive substrate, embodying a single uniformly doped silicon layer having a resistivity of 10 – 20 Ω-cm. The absence of low resistive path between different parts of the die offers higher flexibility in reducing digital noise coupling at the layout stage of mixed-signal chip design.

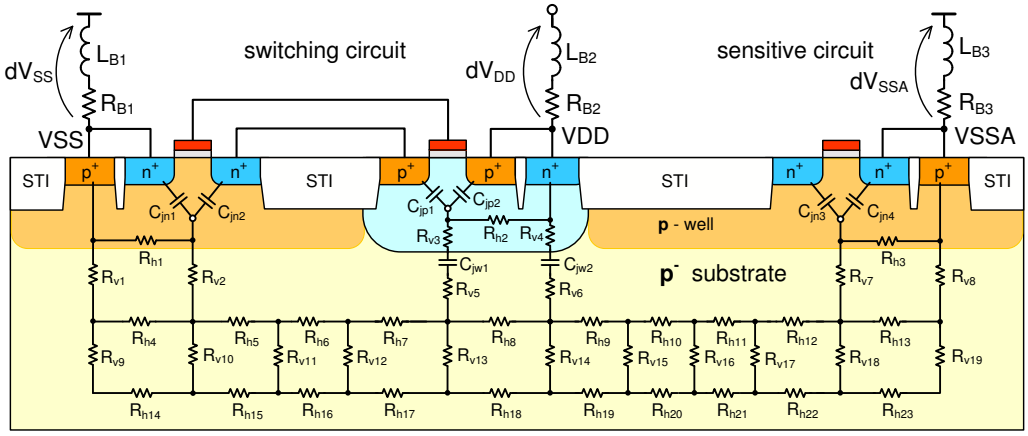
In triple-well technology n-type buried layer breaks the resistive path from the digital noise source to the analog circuits, serving as a blocking feature when using separate ground and supply buses [Larsson 01]. Such cheap technological add-on

efficiently reduces cross talks between analog and digital circuitry in mixed-signal ICs.

Mixed-signal circuits fabricated in a SOI substrate, see Fig. 3.6(d), show better performance than circuits implemented in bulk CMOS processes. Since each transistor capacitively isolated from the other devices, SOI gives high isolation between different circuit areas for low frequencies [Backenius 07]. In spite of the higher manufacturing cost of SOI technology comparing to bulk CMOS, it is believed to be extensively used in future for low power mixed-signal designs [Fukuda 01].



(a)



(b)

Figure 3.7: Lumped element substrate model of a mixed-signal circuit fabricated in (a) – epitaxial substrate, (b) – high resistive substrate

In Fig. 3.7 lumped element representation of epi- and high resistive twin well substrates is given [Owens 05]. Separate analog-digital power supply network scheme is assumed in the model. Capacitors C_{jni} and C_{jpi} (index i represents any integer number), connected to the bulk terminal of a transistor, represent source/drain-bulk junction capacitances and usually included into transistor model.

In [Su 93] it was experimentally stated and illustrated by means of simulations

that high doping concentration of p^+ bulk in epitaxial technology makes it acting like a single node. Current flow lines from or to the active chip domain go vertically through the epi layer into the p^+ bulk. The amount of lateral current flow is negligible, around 5% (such assumption, however, is valid only when switching and sensitive parts are separated by more than 4 times the epitaxial layer thickness, i.e. 16 – 28 μm, otherwise horizontal current flow must be taken into account [Su 93]). Resistors R_{ei} model these physical processes – switching current flows directly to the heavily doped bulk node and spreads there independently on the physical distance between noise source and noise sensor. Note that this node is floating with respect to entire chip ground (it is not tied to the ground). Backside connection is possible only when the bulk resistance is very low, less than 0.006 Ω-cm [Roermund 04]. In this case low inductive connection to the leadless packages or gluing to the board ground is possible resulting in a very low digital noise coupling. In the model only the case of floating bulk is assumed.

Knowing active elements geometry values of resistors R_{ei} can be calculated [Su 93]:

$$R_{ei} = \left(\frac{k_1 \rho T}{(L_i + \delta)(W_i + \delta)} \right) \| \left(\frac{k_2 \rho}{2(W_i + L_i + 2\delta)} \right), \tag{3.14}$$

where T – effective epitaxial layer thickness, L_i and W_i are length and width of diffusion area, ρ is the resistivity of epitaxial layer, and k_1, k_2, δ are technology dependent parameters.

N-well–epitaxial layer junction capacitances C_{jwi} can be defined if doping concentrations and well geometry is known [Sze 81]. Since transistor geometry (length and width for each diffusion area) could easily be defined before the final layout of the circuit is done, it is possible to build rough lumped element substrate model at schematic stage of the design for predicting substrate noise performance of the system.

Possessing pretty much similar surface structure as epi-technology, deep structure of high resistive substrate differs significantly from that in heavily doped substrate, see Fig. 3.7(b). In contrast to heavily doped substrate, distributed nature of lightly doped silicon [Soens 05] makes mixed-signal behavior very layout dependent – model parameters cannot be predicted until the final layout of the circuit is obtained. Furthermore, extracted lumped element model will be much more complicated, resulting in inadequate simulation time and accuracy in case of the large circuit. A practical way for substrate extraction is boundary element method [Brandtner 02].

Majority of open literature sources considering coupling effects in integrated mixed-signal systems focus on practical methods of digital noise coupling reduction, which are verified on simplified structures or complicated mixed-signal ICs.

The efficiency of *power supply network separation* was already demonstrated in Section 3.2. Reported in [Larsson 01] measurements of rms jitter of three inte-

grated PLLs featuring various power supply schemes show significant difference in device performance. The phase-locked loop with separate VSS and VDD exhibited twice less amount of jitter than that with the shared supply networks. A PLL with separate VDD but shared VSS demonstrated even better noise performance; such behavior, however, is caused by high sensitivity of loop filter MOS capacitors to the substrate noise. Replacement of semiconductor capacitors by MIM capacitors will probably result in reduced rms jitter for separate VSS and VDD configuration.

Adding on-chip *decoupling capacitors* between supply and ground buses, see Fig. 3.8, is an efficient and wide spread method for switching noise influence minimization. In analog subcircuits decoupling capacitors together with bond wire inductance form low pass filter which suppresses voltage perturbations at the supply network. Blocking capacitors used in digital parts serve as a current source for generated current spikes – most of the supply AC current flows into decoupling capacitors instead of bond wires, thus quieting $VDD - VSS$ voltage. Care must be taken when using high quality blocking capacitors, since LC-tank formed by inductance L_B and capacitance C_d could cause unwanted oscillation in the supply network. To avoid this parasitic effect resonant tank is damped by placing resistors R_d in series with blocking capacitors [Larsson 98]. Widely used as the decoupling capacitors MOS transistors already have finite channel resistance which is enough for damping the LC network [Larsson 97]. Despite the fact that MOS capacitors offer sufficient dumping of the supply network and have high capacitance per unit area, care must be taken when using them for blocking digital networks, since they could become a path for di/dt noise injection into the substrate. For this reason PMOS transistors fabricated in a well are preferable as a decoupling capacitors. Junction capacitance will prevent low frequency components to be injected into the substrate. As an alternative, MIM capacitor formed with upper metallization layers having low parasitic capacitance to the substrate could be used for decoupling digital subcircuits, and active PMOS capacitor in a n-well for decoupling sensitive blocks.

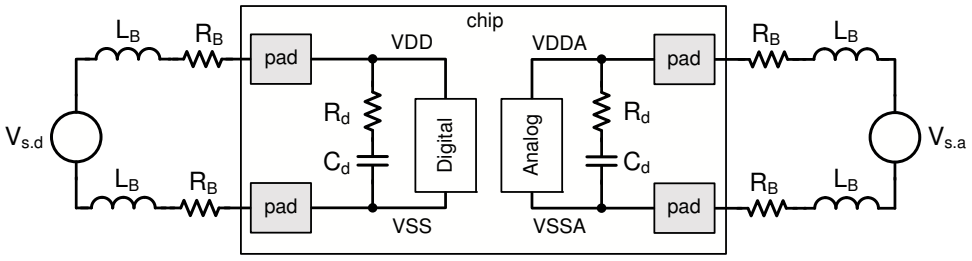


Figure 3.8: Decoupling capacitors added to supply networks

Layout level methods described in two previous paragraphs are used for reducing voltage perturbations at supply buses of the IC. Another set of layout considerations are aimed at improving electrical isolation between different domains of

the chip. In [Su 93] empirical study of noise transfer in lightly doped substrate showed, that coupling decreases linearly with the *separation distance*. At the stage of floorplanning, placing the most sensitive blocks at the largest distance from switching circuitry decrease the amount of coupled noise. This method, however, is not efficient if highly doped substrate is used.

In lightly doped substrate a *guard ring* placed around analog part creates a low impedance path to ground potential, thus reducing the noise coupled from distant domains. Among several different guard ring configurations, dual ring (shown in Fig. 3.9) formed by p^+ substrate contact and n-well ring surrounding the former is among the most efficient protector [Chen 00]. Another benefit of using n-well structure is that it breaks heavily doped p-well path, where the density of current lines is higher than in lightly doped substrate. This further increases the impedance between the noisy and sensitive parts of the chip. Fig. 3.9 also illustrates alternative way of breaking conductive upper layer – using moat mask. Blocking of p-type implant by means of moat mask exhibits more effective isolation in state-of-art CMOS technologies than n-well guard ring [Roermund 04].

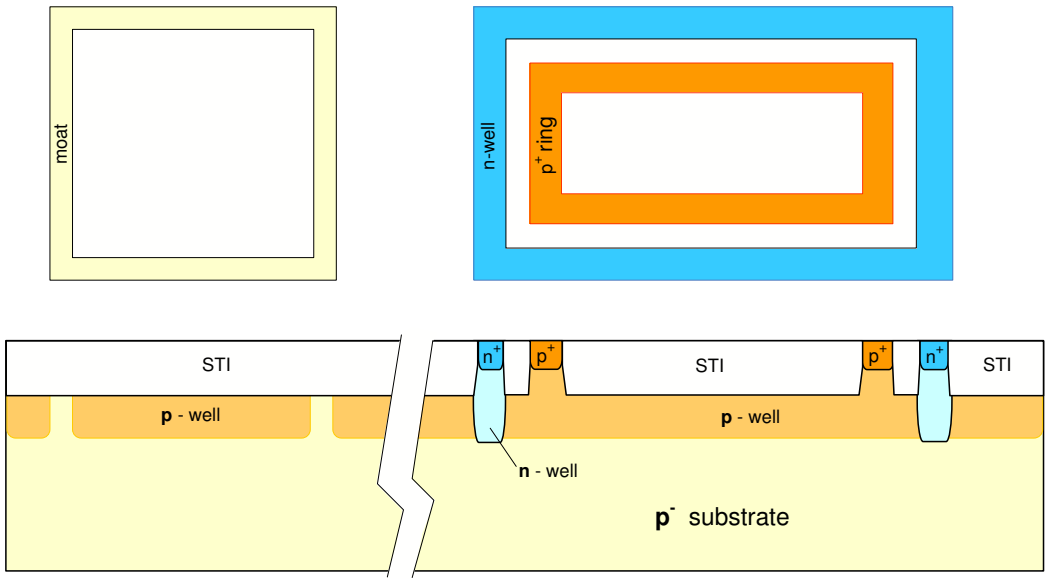


Figure 3.9: Moat and guard ring substrate isolation

Even with the gap in a p-well, resistive path still exists between NMOS transistors on different parts of the die. $P-n$ junction formed by the n-well and a bulk performs effective low frequency noise isolation. Depending on the area of n-well significant attenuation could be achieved at frequencies up to several hundred megahertz [Yeh 04]. This is a reasonable frequency range for phase-locked loop devices since spectral content of most supply perturbations contains reference frequency (usually not exceeding 70–80 MHz) and its harmonics. In a standard CMOS process protection by means of $p-n$ junction is possible if a circuit is

designed using only PMOS transistors. *Triple-well technology* cancels this limitation (Fig. 3.6(c)). Patrik Larsson in [Larsson 01] reported a comparative analysis of PLLs fabricated in standard and triple-well technologies. The PLL placed in a $p-n$ junction-separated well remains almost unaffected by on-chip switching circuit and demonstrated superior noise performance than the PLL fabricated in a twin well technology. It was also shown that isolation efficiency is very dependent on the well area.

As it was mentioned in Section 3.2 *circuit level techniques* should be considered to reduce switching noise at supply buses of the chip. Providing a number of very important advantages over the other logic families (low power consumption, high integrity, good scalability) CMOS logic could hardly be replaced by the other low-noise logic types in complex digital circuits such as sigma-delta modulator or prescaler. However, for some blocks CMOS implementation should be avoided. Digital buffer driving high capacitive load is the example of such block. For measurement purposes it is sometimes required to route a digital signal, switching, for instance, with a reference frequency, to the output (lock time measurement can be performed by measuring period deviation of a feedback signal from the reference source). Fig. 3.10(a) shows a schematic realization of CMOS digital buffer driving a capacitive load C_L. High supply current peaks transformed into the voltage perturbations at VSS bus couple into the substrate and become a source of large reference spurious tones at the high frequency output signal of the PLL.

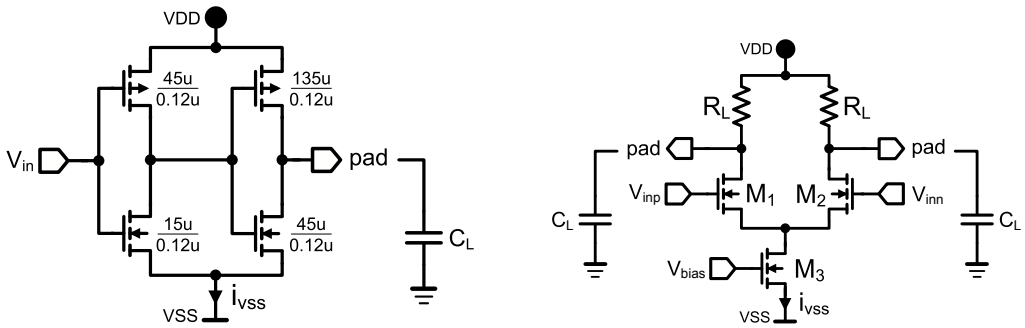
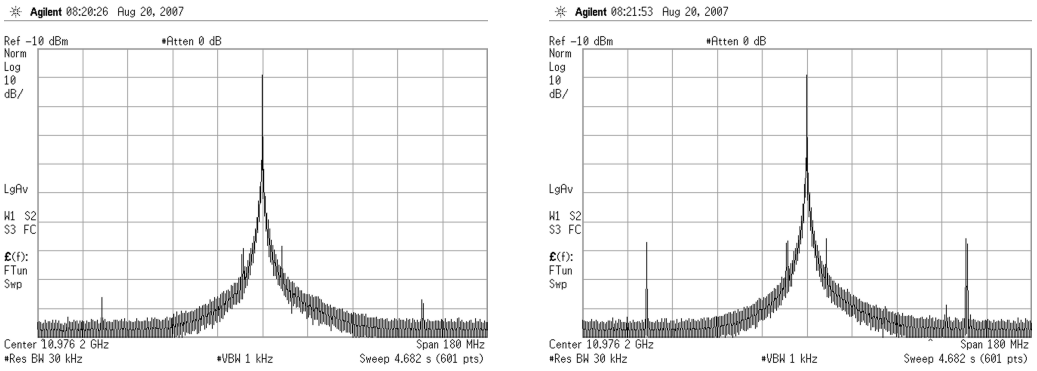


Figure 3.10: Output digital buffers (a) – CMOS, (b) – CML

For test purposes the buffer illustrated in Fig. 3.10(a) was implemented in an integrated synthesizer. With the disabled buffer PLL exhibited reference spurious tones with a power of –76 dBc at frequency offset of 64 MHz apart from the carrier, see Fig. 3.11(a), whereas enabled buffer increased reference spurs by 20 dB (Fig. 3.11(b)).

Such performance degradation can be avoided if current-mode logic (CML) buffer is used as a pad driver. In Fig. 3.10(b) circuit diagram of a CML buffer is shown.



(a) (b)

Figure 3.11: Measured output spectrum of a fully integrated PLL with a digital buffer shown in Fig. 3.10(a): (a) – with disabled buffer, (b) – with enabled buffer

Current source M_3 specifies the current i_{VSS} through the ground and keeps it constant during the switching. In reality i_{VSS} will still contain some transitions because of the finite output impedance of a current source M_3, but they will be significantly weaker than in CMOS output buffer. In Fig. 3.12 the derivative of supply currents, obtained after simulation of CMOS and CML buffers is illustrated. Both buffers are driving the capacitive load $C_L = 10$ pF. CML buffer exhibits more than five times lower peak values of di_{VSS}/dt than CMOS buffer. Current-mode logic buffers suffer from one significant disadvantage: the output voltage swing will never be as high as in CMOS buffer and sometimes additional external voltage amplifier is required.

Among the other known techniques for supply noise reduction are active reduction technique [Liu 99] and supply current shaping method [Badaroglu 05], which however did not find widespread use in integrated frequency synthesizers.

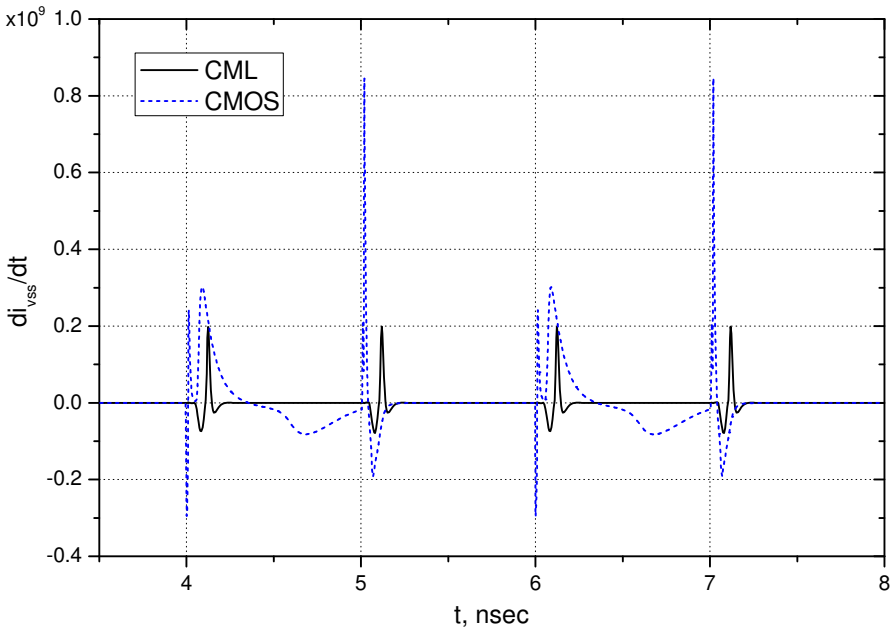


Figure 3.12: Time derivative of the supply currents of CMOS and CML buffers

Chapter 4

Integrated Sigma-Delta Modulators for Frequency Synthesis Applications

4.1 Characteristics of Sigma-Delta Modulators

Digital sigma-delta modulators can be characterized by the following set of parameters important for frequency synthesis applications.

Order. The z-transform of modulator's output signal $Y(z)$ can be represented as

$$Y(z) = A(z)H_{STF}(z) + e(z)H_{NTF}(z), \tag{4.1}$$

where $A(z)$ – input signal, $e(z)$ – quantization error, $H_{STF}(z)$ and $H_{NTF}(z)$ are signal and noise transfer functions respectively.

The noise transfer function is a scope of interest in sigma-delta modulator since it defines the shape of quantization noise distribution over the frequency. In general, noise transfer function is written as [Schreier 04]

$$H_{NTF}(z) = \frac{\sum_{k=0}^{M} b_k z^{-k}}{\sum_{k=0}^{N} a_k z^{-k}} \tag{4.2}$$

The maximum power of complex variable z determines the order of sigma-delta modulator. Quantization noise distribution defined by the $H_{NTF}(z)$ maps to the phase noise of the sigma-delta synthesizer. Very often modulator's order comes in agreement with PLL order – usually it does not exceed loop filter order. However, its not a requirement and tradeoffs are possible.

Number of stages is equal to the number of quantizers in the modulator. Single stage (or single loop) sigma-delta modulator incorporates one quantizer, while multiple stage modulator (referred as a MASH [Matsuya 87]) consists of several single loop devices combined by a linear network. MASH architecture allows to build stable sigma-delta modulator independently on its order. Recently, reduced complexity multistage modulator was reported in literature, in which all stages are connected in series with each other and it does not incorporate linear network for combining the stages [Bornoosh 05]. Empirical study of different architectures showed that MASH modulators generate higher decorrelated output sequence than single-loop modulators of the same order and output resolution, resulting in a better spurious performance when used in the frequency synthesizers [Muer 02]. Another advantage of MASH modulators when operating in mixed-signal integrated systems is their simple hardware implementation and ease of scaling. However, single-loop modulators offer more flexibility in choice of noise transfer function and output signal resolution. At the moment, third order single-loop and MASH 1-1-1 (three stages of first order each) modulators are the most widely implemented architectures in modern high frequency sigma-delta phase-locked loops.

Input range defines as the range of static input signal for which stable operation of modulator is assured [Norsworthy 97], [Schreier 04]. Because of the essential stability, MASH and low order single loop modulators offer full operation range. High order single loop modulators often have reduced input range. The basic mechanisms of stable input range extension are the proper choice of modulator transfer function and quantizer resolution. For frequency synthesis applications, where only digital DC input is applied to the modulator, the range of safe operation can easily be verified by means of simulation for all possible input combinations. The use of modulator with limited input range together with a PLL results in the reduced division ratio range.

Output resolution, which usually matches the resolution of quantizer, sets the lower limit for the modulus number in prescaler – number of division ratios must be at least 2^d, were d denotes the output resolution of a modulator. MASH is inherently multibit architecture, while single-loop modulator can comprise either one-bit or multiple bit output. The main PLL performance issues strongly influenced by the resolution are spurious tone power and quantization noise folding caused by the nonlinearities in phase-frequency detector and charge pump. Empirical studies of different sigma-delta modulator architectures showed, that single bit devices are more tonal than their multibit counterparts even when dithering is applied [Norsworthy 97]. The biggest advantage of single bit (two quantization levels) modulators is high immunity against nonlinearities introduces by the PLL. This fact has very simple explanation: two points are enough to define only a linear function. With the number of output levels more than two, quantization noise will be effected by the nonlinearities of a loop before mapping to the output phase noise. For example, 3-bit (8-level) MASH modulator is very sensitive to

nonlinearities and even small distortions result in appearance of significant noise floor which degrades the phase noise at close to the carrier offsets. Hence, special care must be taken in analyzing nonlinear properties of the PLL when multibit sigma-delta modulator is used.

High order multibit modulators impose a limitation on frequency dividers: as illustrated in Fig. 4.1, average division ratio range can be significantly smaller than instantaneous division ratio range. For example, 8-modulus divider with the ratios $N, ..., N+7$ controlled by the 3-rd order, 3-bit output MASH could generate average division ratios between $N+3 \leq N_A < N+4$, while modulator's sequence spreads over all 8 division ratios. For wideband applications such small frequency range ($\Delta f_{out} = f_{ref}(N+1-N) = f_{ref}$) is often insufficient and divider modulus extension is required.

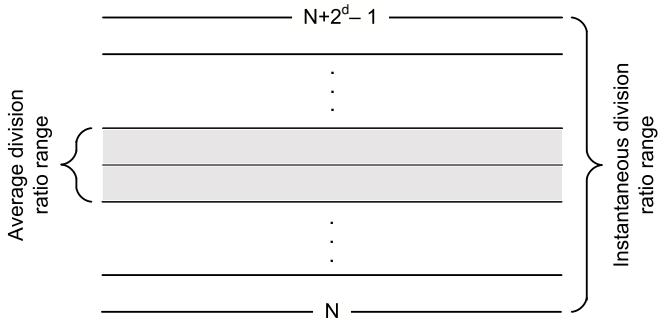


Figure 4.1: Average division ratio of a divider controlled by multibit modulator

Input resolution determines the accuracy of output frequency tuning. The higher the resolution, the bigger the number of output frequencies within the locking range can be generated (however, when PLL is synchronized by commercial quartz oscillator, theoretically achieved frequency resolution could lie in the range of frequency error provided by the reference oscillator). High resolution (more than 20 bits) high order undithered modulators are able to generate almost tone free sequences, when proper control signal or initial conditions are applied [Miller 91] (fractional spurs still exist, but their density is as low as $f_{ref}/2^{20}$, practically less than 100 Hz, which can be treated as a phase noise). Resolution specifies the capacity of storage and adding elements, thus defining the size and current consumption of the modulator. Therefore, the input resolution should not exceed too much the limit necessary to meet frequency step specifications.

Applied spurious reduction technique. A well known problem of the digital sigma-delta modulators is their tendency to generate limit cycles with a short repetition period when a constant digital signal is applied to the input. Periodic quantization error generated by the device in such conditions has spiky spectrum, resulting in a spurious signals at the high frequency output of the PLL.

A set of techniques aimed at improving tonal behavior of the sigma-delta modulators were reported in literature and found a use in practical devices [Norsworthy 97],

Table 4.1: Sigma-delta modulators in monolithically integrated synthesizers

Reference	**Technology**	**ΣΔ modulator architecture**	**ΣΔ input resolution**	**% of area occupied by modulator**
[Hegazi 03]	0.35 μm CMOS	MASH 1-1-1 with dithering	16-bit	5 %
[Lee 04]	0.5 μm BiCMOS	4-th order single-loop	21-bit	9.4 %
[Perrott 97]	0.6 μm CMOS	MASH 1-1	16-bit	5.2 %
[Tiebout 04]	0.13 μm CMOS	2-nd order single-loop	16-bit	3.4 %
[Shu 03]	0.35 μm CMOS	3-nd order single-loop	–	28.5 %
This work	0.13 μm CMOS	MASH 1-1-1 with dithering	11-bit	3.2 %

[Borkowski 05]. A low-cost and easy to implement method for whitening the quantization noise spectrum of the sigma-delta modulators is based on loading predefined initial conditions. Quantization error spectrum can be smoothed when irrational initial conditions are loaded to the integrators of the device. Unfortunately, real digital modulators commonly used in fractional-N frequency synthesizers have limited bit resolution, which makes the use of irrational numbers impossible.

Sigma-delta modulators tonal performance is known to be input dependent, bringing an alternative to loading initial conditions – applying proper input values. These two methods give very similar result, only that the latter also could influence the DC component of the quantized signal, yielding a small frequency shift when the modulator controls fractional-N PLL. By applying predefined initial conditions and controlling input signal level, periodicity of the quantization error can be significantly reduced, but still not eliminated.

An effective widespread method for smoothing quantization error spectrum and reducing the dependence of tonal performance on the input signal is dithering [Chou 91]. The result is obtained at expense of additional hardware.

Occupied chip area and power consumption are the last but not the least parameters of sigma-delta modulators considered in the work. Area is almost linearly proportional to the input resolution and strongly depends on the modulator's order, architecture, and schematic implementation of logic gates. Table 4.1 summarizes modulators' characteristics of some modern sigma-delta PLL designs (for calculation of the area occupied by sigma-delta modulator test pads of the chips were not taken into account).

Fig. 4.2 shows idealized voltage and current waveforms at supply terminals of

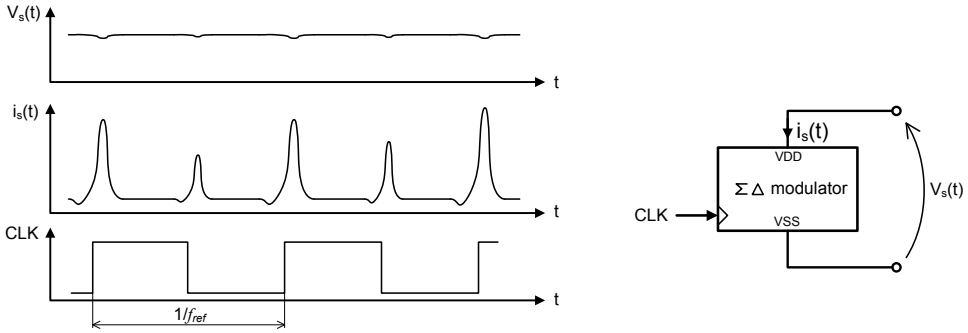


Figure 4.2: Power supply waveforms in sigma-delta modulator

the sigma-delta modulator implemented in CMOS logic. Current spikes occur at clock edges; during the rest time of operating period supply current is very small. Instantaneous power consumed by the device is

$$P(t) = V_s(t) \cdot i_s(t) \tag{4.3}$$

Average (or effective) power defines as

$$P_{avg} = \frac{1}{T} \int_0^T P(t)dt, [W], \tag{4.4}$$

where T is some integration interval.

Since CMOS circuits consume most of the current during clock transitions, effective power consumption is dependent on clock frequency. In order to express power efficiency independently on the triggering frequency, a term "energy consumed per one operation" is introduced. The total energy consumed by the circuit within a time interval T:

$$W_T = P_{avg} \cdot T, [J] \tag{4.5}$$

If N transitions of triggering signal fit in the internal T, then the amount of energy consumed per one operation is

$$W_{op} = \frac{W_T}{N} = \frac{P_{avg} \cdot T}{N} = P_{avg} \cdot T_{ref} = \frac{P_{avg}}{f_{ref}}, [J/operation] \tag{4.6}$$

Obviously per-operation energy depends on the state of logic element and signals applied to it [Stojanovic 99]. Therefore an input digital pattern specific for the circuit and operating conditions is applied to the device, and average energy is calculated. Practically, W_{op} is obtained by simulation of logic cell over some interval and calculating effective power consumption of the circuit. For instance, Michael Perrott in [Perrott 97] gives calculated energy consumption per

Table 4.2: Sigma-delta PLL performance tradeoff

Performance issue		**ΣΔ modulator architecture/specifications**
Fractional spurs power	high	Low order
		Single bit output
	low	High order, miltibit output
Sensitivity to nonlinearities	high	Multibit output
	low	Single bit output
Input range	full	MASH modulator with first order stages
		Single loop, multibit output
	reduced	Single loop, high order, single bit output
Frequency step	large	Low input resolution
	small	High input resolution

operation for different circuit implementations of modulator's blocks. This helps to determine power consumption of the whole modulator and choose the most power-efficient implementation.

Since the scope of this work is monolithically integrated sigma-delta synthesizers, not only the average energy consumption of modulator is of interest, but also amplitude of current spikes generated at power terminals of the device. The importance of peak to average supply current ratio reduction is expanded in Section 3.

Finally, in order to conclude the section, Table. 4.2 is presented. Here some PLL performance aspects able to be achieved with specific modulator architectures are summarized.

4.2 Choice of Modulator Architecture

In spite of the big variety of modulator architectures, the choice of specific topology for the use in fractional-N PLL is limited. In sigma-delta PLLs third order modulators are commonly used. The lower order modulators are not able to generate tone-free digital sequence, while the higher order topologies produce powerful quantization noise, which can hardly be suppressed by the loop.

In general, single loop implementations are more complex than their multiple loop counterparts [Muer 02]. Since the work focuses on the hardware efficient implementations of integrated sigma-delta modulators single loop architectures are not considered.

Third order multi-stage modulator can be implemented as MASH 1-1-1, MASH 1-2, and MASH 2-1 structure. The latter two topologies comprise second order stage. All three topologies have similar hardware complexity [Sun 99], lower than single loop modulators, which makes them beneficial for compact, low cost designs. Undithered MASH 1-2 and MASH 2-1 structures are able to generate less

tones than MASH 1-1-1 modulator, but they suffer from one significant disadvantage: since they contain a second order stage, which is known to have reduced stable input range [Schreier 04], they are able to cover only the part (around 75%) of the whole fractional division ratio range.

MASH 1-1-1 structure appears to be one of the best choices for on-chip modulator because of the ease of implementation, stability over the whole input range (which results in the absence of gaps in the generated high-frequency LO signal), tone-free output sequence in the case when proper dithering is used, and third-order shaped quantization noise. At the moment, MASH 1-1-1 is the most widely used structure in integrated sigma-delta frequency synthesizers.

A comparative study of different sigma-delta modulator's topologies for frequency synthesis applications is given in [Xiaojian 07].

4.3 General Structure of a Sigma-Delta Modulator

In general, digital sigma-delta modulator is a feedback system containing loop filter and a uniform quantizer. There are various ways of representing modulator's topology differing by the number of feedback and feedforward paths and loop filter structure [Schreier 04]. Due to the leakage and nonlinearities inherently presented in continues time analog sigma-delta modulators, each topology can offer specific advantages and disadvantages. However, for all-digital sigma-delta modulators operating with fixed point arithmetics, each topology can be implement as algebraically equivalent structure offering the same functionality. Some topologies of digital modulators gained popularity because of the ease of implementation.

For the further analysis of sigma-delta modulators, two topologies shown in Fig. 4.3 are considered: single feedback topology [Schreier 04] and error-feedback structure [Cutler 60].

The output for a single feedback modulator in z-domain is given by

$$Y(z) = \frac{H(z)}{1 + H(z)} A(z) + \frac{1}{1 + H(z)} e(z) \tag{4.7}$$

Defining signal transfer function and quantization noise transfer function as

$$H_{STF}(z) = \frac{H(z)}{1 + H(z)}, H_{NTF}(z) = \frac{1}{1 + H(z)} \tag{4.8}$$

(4.7) transforms into

$$Y(z) = H_{STF}(z)A(z) + H_{NTF}(z)e(z) \tag{4.9}$$

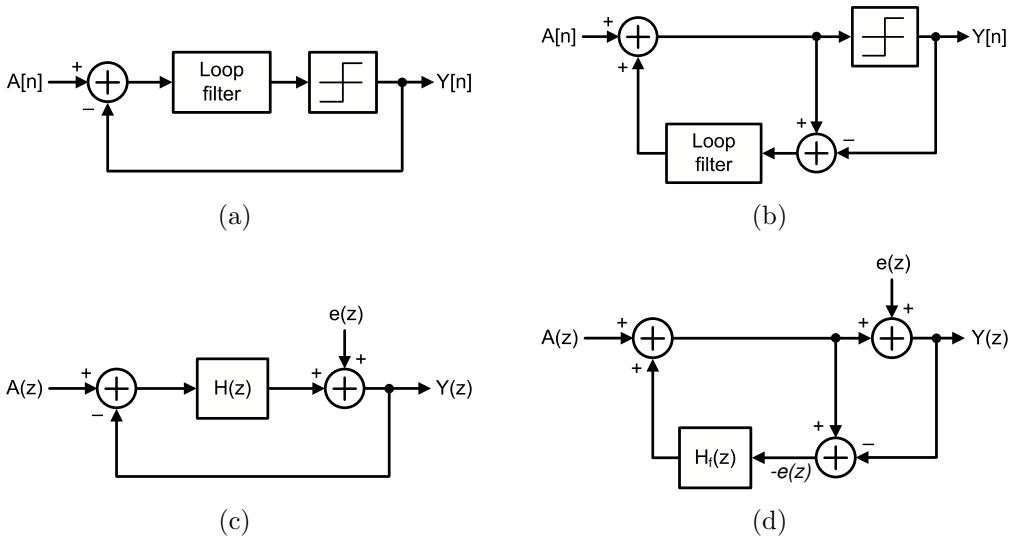


Figure 4.3: Topologies of sigma-delta modulators (a) – single feedback topology, (b) – error-feedback structure, (c) – linear model of a single feedback modulator, (d) – linear model of an error-feedback modulator

The output of an error-feedback structure is given by

$$Y(z) = A(z) + (1 - H_f(z))e(z) \tag{4.10}$$

or

$$Y(z) = H_{STF.f}(z)A(z) + H_{NTF.f}(z)e(z), \tag{4.11}$$

where

$$H_{STF.f}(z) = 1, H_{NTF.f}(z) = 1 - H_f(z) \tag{4.12}$$

are signal and noise transfer functions.

In order to make error-feedback and single feedback structures functionally equivalent, the following equality must be satisfied:

$$H_{NTF}(z) = H_{NTF.f}(z) \tag{4.13}$$

After substituting (4.8) and (4.12) into (4.13) and rearranging we obtain:

$$H(z) = \frac{H_f(z)}{1 - H_f(z)} \tag{4.14}$$

or correspondingly

$$H_f(z) = \frac{H(z)}{1 + H(z)} \tag{4.15}$$

Note that models in Fig. 4.3(c) and Fig. 4.3(d) are not fully equivalent – the signal transfer function is different. In order to make these modulators physically realizable $H_f(z)$ and $H(z)$ must comprise at least one clock delay. Thus, in the error feedback structure input signal goes to the output without delay, while in the single feedback modulator it must be delays for at least one cycle.

4.4 First Order Sigma-Delta Modulator

In spite of the number of significant drawbacks of the stand-alone first order digital sigma-delta modulator, it is still widely considered as a part of more complex multistage modulators extensively used in fully integrated sigma-delta PLLs.

First order sigma-delta modulator comprises a first order integrator as a loop filter. A device which implements the functionality of a first order modulator is a digital accumulator. State space representation of the accumulator is given by (2.2) and (2.3). An overflow terminal serves as an output of the one-bit quantizer. Regardless of the conceptual equivalence of a first order single feedback quantizer and accumulator there are several minor differences between them [Riley 93]. One of the most important is: the input and, consequently, quantized signal in a modulator usually assumed to fall into the range of ± 1, while accumulator generates the output between 0 and 1. Moreover, further observation of accumulator's state space representation leads to another conclusion: quantization error is always negative or equals zero, namely

$$e[n] \leq 0 \tag{4.16}$$

Indeed, since

$$e[n] = Y[n] - A[n] \tag{4.17}$$

and assuming that $0 \leq A[n] < 1$, from (2.2) and (2.3) it implies, that $Y[n] \leq A[n]$, which directly leads to inequality (4.16).

4.4.1 Linear Model

The linear model of a first order modulator is shown in Fig. 4.4.

Digital integrator's transfer function is given by

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{4.18}$$

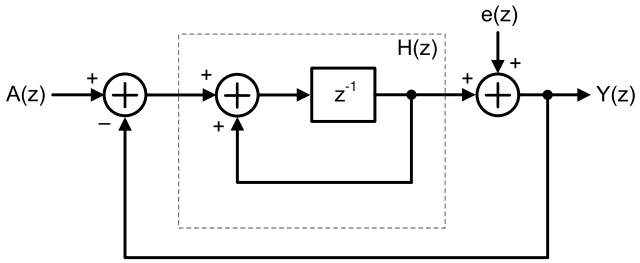


Figure 4.4: Linear model of a first order sigma-delta modulator

Substituting into (4.7), the output in z-domain will be

$$Y(z) = A(z)z^{-1} + (1 - z^{-1})e(z) \tag{4.19}$$

Thus, noise transfer function of a first order modulator is

$$H_{NTF}(z) = 1 - z^{-1} \tag{4.20}$$

Since considered sigma-delta modulator is applied to the frequency synthesizers, the quantization noise should be mapped to the synthesizer phase noise. Two-sided power spectral density of a noise introduced by the sigma-delta modulator into the PLL is given by [Miller 91]:

$$\phi^2_{sdm}(f_m) = \frac{\pi^2}{3f_{ref}} \frac{\left| H_{NTF}(e^{\frac{j2\pi f_m}{f_{ref}}}) \right|^2}{\left(2\sin\frac{\pi f_m}{f_{ref}}\right)^2}, 0 \leq f_m \leq \frac{f_{ref}}{2} \tag{4.21}$$

Substituting noise transfer function into the generalized formula for modulator's noise spectral density (4.21), the PSD of a first order modulator is obtained:

$$\phi^2_{sdm}(f_m) = \frac{\pi^2}{3f_{ref}} \tag{4.22}$$

Thus, phase noise introduced into the PLL has white distribution. The obtained PSD of modulator's quantization noise is substituted into the linear model of a PLL to calculate the total phase noise of the system.

4.4.2 Nonlinear Performance

Under nonlinear performance tonal behavior and quantization noise folding due to the PLL nonlinearities is considered. Since first order modulator generates single-

bit output, the phase noise degradation caused by the nonlinear PLL action is not the case for this architecture.

First order sigma-delta modulator suffers from very poor tonal performance, thus introducing severe fractional spurs into the carrier of the PLL. This makes the use of a standalone first order modulator in a fractional-N PLL inefficient.

The power and the number of tones generated by the first order sigma-delta modulator depends on the modulator's resolution, applied input signal, and initial conditions [Borkowski 05]. The number of tones appeared within a frequency range $[0; f_{ref}]$ in a k-bit undithered modulator equals

$$2^{k-n_a-1}, 0 \leq n_a \leq k-1, n_a \in N \tag{4.23}$$

where n_a is a first active bit starting from the least significant bit of the input static digital signal $A[n]$ (see Fig. 4.5). Note, that equation is true only for zero initial conditions. The higher the number of tones, the lower their peak power (the average power remains constant).

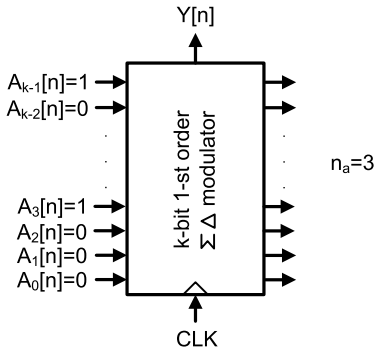


Figure 4.5: Static signal applied to the first order modulator

From (4.23) its obvious that the largest output sequence (the highest number of tones) is generated when the least significant bit is active, i.e. $n_a = 0$. Moreover, if $A_0[n] = 1$ tonal distribution does not depend on the initial conditions and modulator demonstrates the best spurious performance. Nevertheless, tones are not distributed uniformly, and powerful harmonic at twice less the clock frequency always present. The PLL controlled by the first order modulator has the lowers spurious at frequency offset $f_{ref}/2^k$ from the carrier.

Dithering – a widespread method for whitening quantization spectrum of the sigma-delta modulators – just slightly helps to improve tonal behavior of the first order modulator [Norsworthy 97].

4.4.3 Hardware Implementation

The most suitable representation of the modulator for efficient hardware implementation is the error feedback structure. The error feedback linear model of the first order modulator in z-domain is shown in Fig. 4.6(a). Loop filter is derived from the model in Fig. 4.4 using (4.15) – as a result filter consists of a unity delay element. The output of a linear feedback structure of a first order modulator in z-domain is

$$Y(z) = A(z) + (1 - z^{-1})e(z) \tag{4.24}$$

and differs from (4.19) by the absence of unity delay of the input signal.

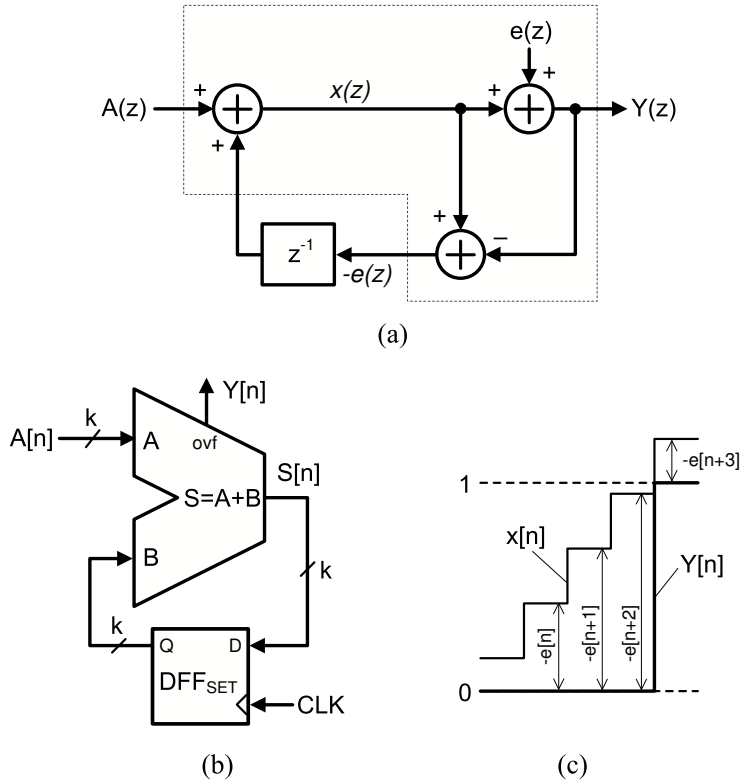


Figure 4.6: (a) – error feedback model of a first order sigma-delta modulator, (b) – hardware implementation of an error feedback model, (c) – quantization error behavior

Digital k-bit adder implements the function of the framed part of the modulator shown in Fig. 4.6(a). The framed part contains a 1-bit quantizer, an adder of the input and feedback signals, and a quantization error generator. Input signal and feedback signal are applied to the inputs of the adder, overflow terminal generates the quantized signal, and calculated sum represents the quantization error with a negative sign:

$$S[n] = -e[n] \tag{4.25}$$

The loop filter is implemented with a k repetitions of the single edge triggered D-flip-flops (DFF_{SET}) as shown in Fig. 4.6(b) (here and further in the work the following notation is adopted, unless otherwise stated: CLK is a differential signal consisting of CLKP and CLKN; the frequency of CLK signal equals reference frequency applied to the PLL).

The waveforms in Fig. 4.6(c) demonstrate the circuit operation. Quantizer of a modulator operates as follows: it generates logical '0' when its input signal falls in the range $0 \leq x[n] < 1$, and logical '1' when $x[n]$ exceeds or equals '1'. A positive sum generated at the output of the adder is equivalent to the quantization error with a negative sign (as it was stated in (4.16), quantization error does not exceed zero level). If $x[n]$ overcomes the unity level, the adder generates an overflow and outputs the value, which equals the residue of division of $x[n]$ by 1.

Fig. 4.7 reveals the detailed structure of a modulator in Fig. 4.6(b). The adder consist of k repetitions of 1-bit full adder (FA) element. The carry-out terminal of each FA is connected to the carry-in port of the following element. Carry-in terminal of the first adder is connected either to logical zero or to logical one. The second connection ensure that the output sequence with the largest period will be generated, independently on the absolute value of signal $A[n]$. Such connection, however, also adds a small DC offset to the input signal, resulting in a PLL carrier frequency shift. The amount of the frequency shift depends on the reference frequency and modulator's resolution k.

There is a big variety of ways to implement the functionality of a full adder in a digital circuitry [Sayed 02], [Jiang 04]. In this work a classical 28-transistor full adder is considered. The circuit diagram is shown in Fig. 4.8.

In order to verify the energy consumption, the adder was simulated in Advanced Design System 2006 environment using the models of transistors for 0.13 μm CMOS technology. The supply voltage is 1.5 V. The sizes of all transistors except those, shown in the diagram are: NMOS – W/L = 0.3μm/0.12μm, PMOS – W/L = 0.5μm/0.12μm (in spite of the fact that technology is named as 0.13 μm CMOS, the minimum drawn gate length is 0.12 μm). As it was mentioned above, energy consumption of a circuit depends on the statistics of the applied input pattern. The input sequence used as the stimulus was as follows: random digital signals were applied to the inputs A and CI; generated sum at the output SO was delayed for one step and applied later to the input B of the full adder. Time dependent sequence to the A terminal is applied with the consideration, that in MASH modulators digital accumulators obtain quantization error of the previous stage as the input, which is changing with time. However, if a 1-st order modulator is used as a standalone device (not as a part of MASH) with a DC signal applied to the input, the power dissipation would be smaller due to the absence of input switching activity. Simulation also showed a strong dependence

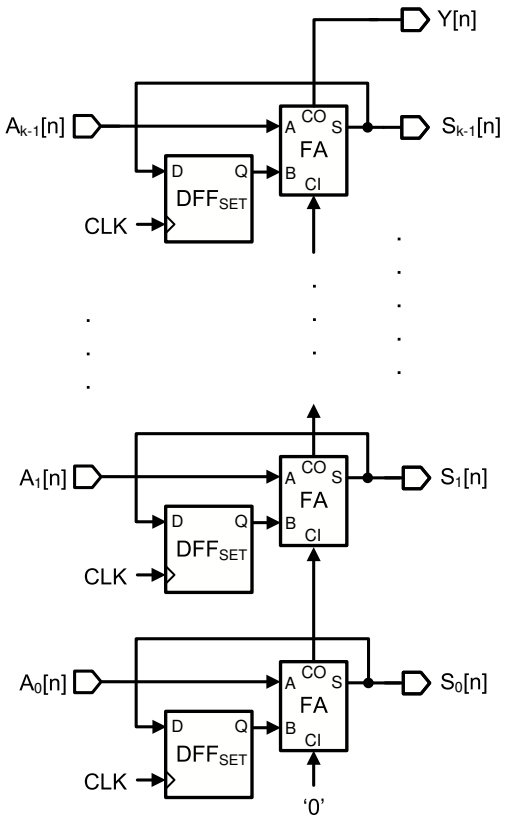
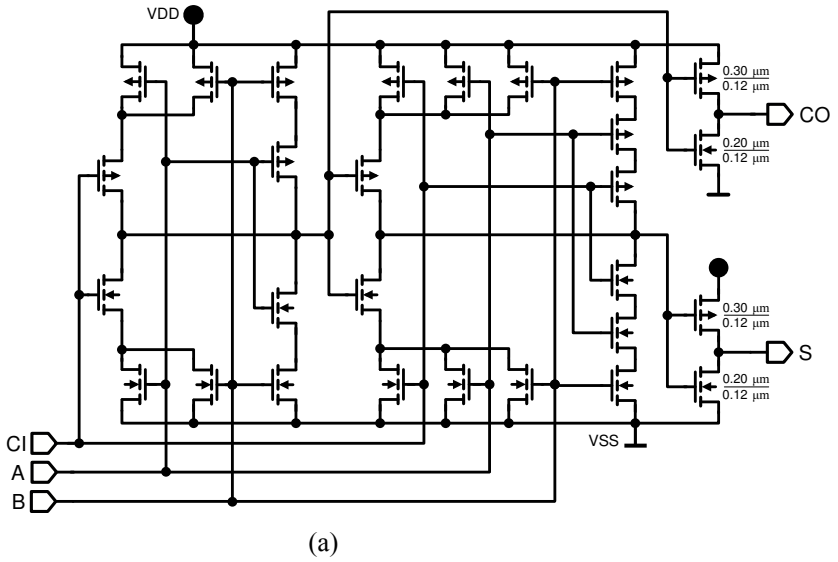


Figure 4.7: Extended representation of a first order modulator structure

of energy consumption on the time shift between the input switching events: if the input signals are synchronized and changing their level simultaneously, consumed energy is twice less than if the input switching events appear at different moments of time. In reality, signals applied to the FA are not synchronized – at B input signal appears just after the triggering signal and the delay introduced by DFF. And only after that, the changes at CI and A take place. For the simulation the worst case is considered, when all input switching events appear at different moments of time. Each output was connected to the inverter, which has approximately the same load capacitance as the stage following the adder in the accumulator, i.e. data input of the flip-flop and carry-in terminal of the full adder. Estimated energy consumption of the full adder is $W_{op} = 17$ fJ/operation.

A single edge triggered D-flip-flop circuit diagram is presented in Fig. 4.9. The flip-flop consists of two latches connected in series. Single edge implies that it is triggered by just rising edge of the clock signal. The sizes of all n-channel transistors are W/L = 0.2μm/0.12μm and p-channel transistors W/L = 0.4μm/0.12μm in all transmission gates and inverters. The flip-flop was simulated using the models of the same 0.13 μm CMOS technology. As an input, a digital random signal with the data rate of 64 Mbit/sec was applied. The frequency of the differential



A	B	CI	S	CO
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
0	0	1	1	0
1	1	0	0	1
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

(b)

Figure 4.8: (a) – full adder circuit diagram, (b) – truth table

clock signal was 64 MHz. Loading capacitance was of the same order as has the input terminal of a full adder. Flip-flop consumed 4.8 fJ/operation.

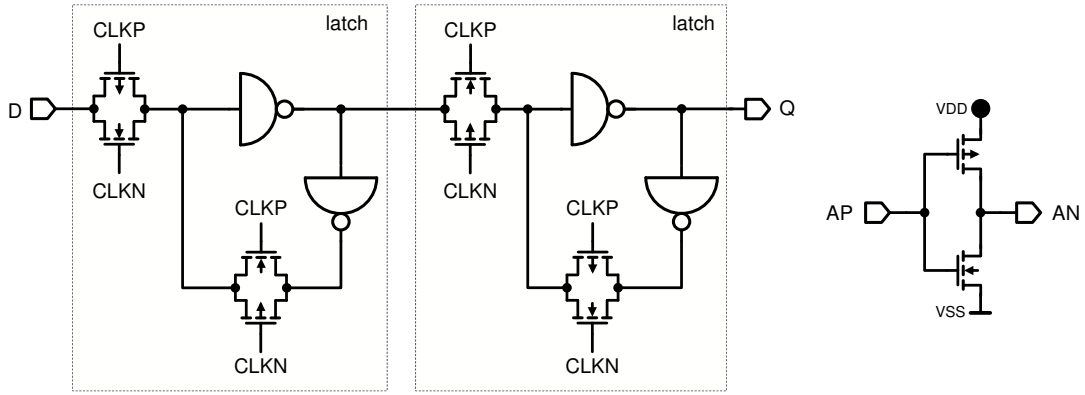


Figure 4.9: (a) – single edge triggered D-flip-flop circuit diagram, (b) – inverter schematic

From the diagram in Fig. 4.7 its obvious that the output of arbitrary stage depends on the carry-out state of the preceding stage. The carry chain propagation delay, which is proportional to the number of FA stages, sets the operation speed limit for the hole accumulator. It can happen that propagation delay for a given resolution is higher than the clock (reference) period, which makes the use of such modulator impossible. A technique called pipelining is used to break the dependence of the adder operation speed on its resolution [Lu 93]. Pipelined first order

sigma-delta modulator is illustrated in Fig. 4.10. The carry bit of each adder is delayed by one clock cycle before applying to the next stage. Corresponding number of D-flip-flops is also added to the input and output to compensate delays introduced in carry path. Not every carry path should be pipelined if a propagation delay of a 1-bit accumulating element is much lower than the reference period. Pipelining can significantly increase the complexity of device. In the worst case when each stage is pipelined, the number of primitive digital gates (FA and DFF) can reach $(k-1)^2 + 2(k-1)$ versus $2k$ in non-pipelined modulator (see Fig. 4.10 and Fig. 4.7).

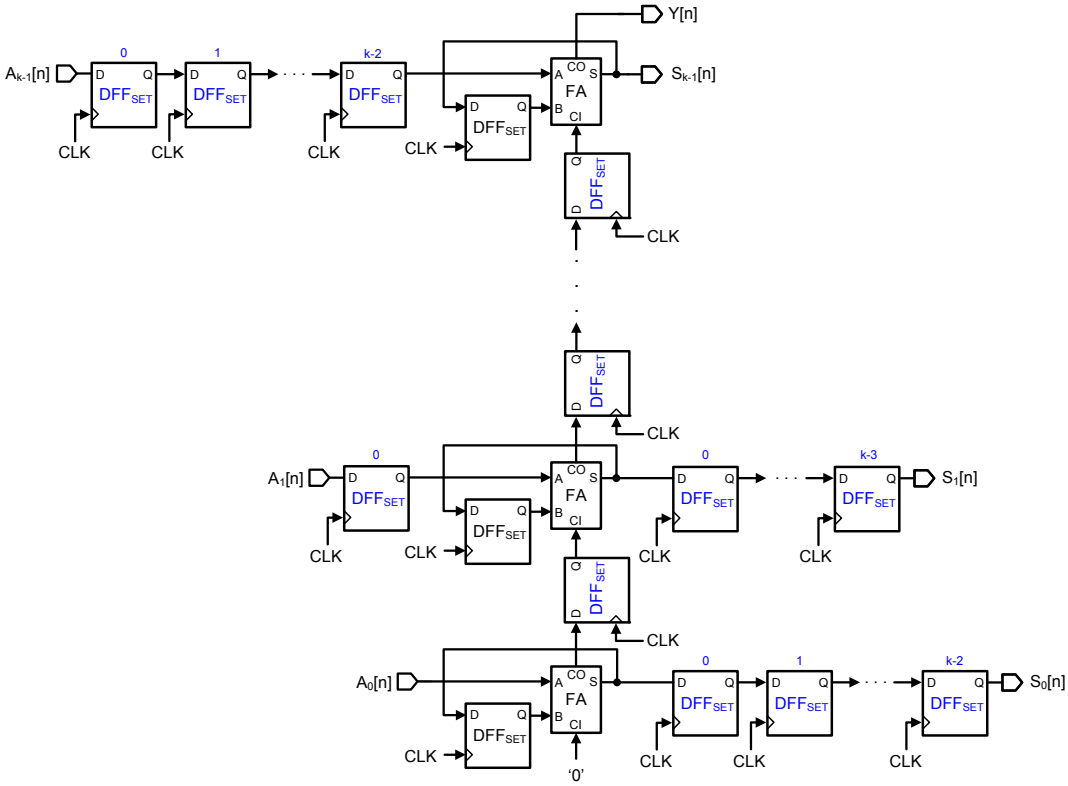
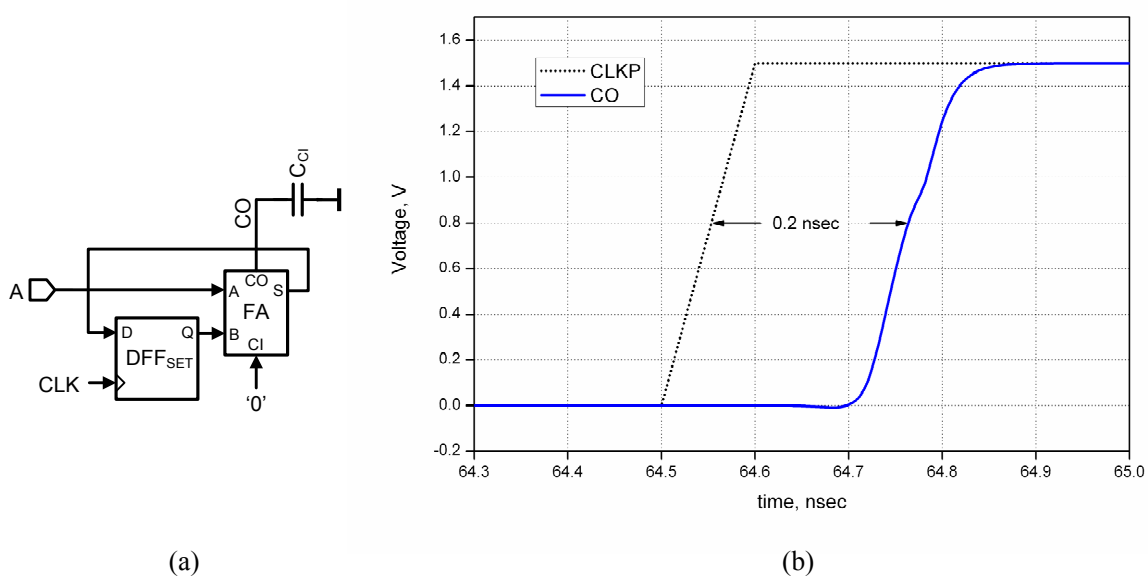


Figure 4.10: Pipelined first order modulator

In order to estimate how many, if any, pipelined levels are required for the first order modulator designed in 0.13 μm CMOS technology, 1-bit accumulating element was simulated. Simulation circuit is shown in Fig. 4.11(a). Capacitance C_{CI} models the input capacitance of the carry-in terminal of FA. Simulated diagram presented in Fig. 4.11(b) shows that propagation delay in a carry path is 0.2 nsec. Taking into account some increase in propagation delay in real device caused by wiring parasitics, delay margin is more than enough to assemble up to 30-bit accumulator operating at 64 MHz clock frequency without pipelining. Since accumulators with resolution exceeding 26-bits are almost never employed in integrated sigma-delta synthesizers, first order modulator also will not be sensitive

to some insignificant reference frequency deviations.



(a) (b)

Figure 4.11: Delay estimation for 1-bit accumulating block: (a) – simulation setup, (b) – simulated waveform

The energy consumption of a D-flip-flop can be decreased. Single edge triggered flip-flop uses just one (rising or falling) edge of a triggering signal to perform the operation. The other edge is functionally useless. As it was mentioned above, most of the power is consumed during the transitions. Since both triggering edges provoke switching of transistors, the power is consumed during both rising and falling clock edges.

The use of dual edge triggered (DET) elements is a well known strategy for reducing clocking power in triggered systems [Unger 81]. The elimination of idle clock edges in such elements allows to decrease the energy consumed per one operation. Dual edge triggered D-flip-flop circuit diagram is shown in Fig. 4.12 [Hossain 94]. It consists of two latches connected in parallel and combined in a single output by means of a multiplexer. Output multiplexer is an additional element which was not presented in DFF_{SET}. In contrast to the implementation cited in [Hossain 94], the signal is inverted twice in the latch before applying to the multiplexer, thus eliminating the necessity of the output inverter. At the rising edge the upper latch saves the input signal and holds it until the falling edge arrives. In the same time multiplexer routs the signal from the upper latch to the output. At the falling edge the second part of the flip-flop operates. Simulated dual edge triggered flip flop operating under the same conditions as DFF_{SET} demonstrated superior energy consumption: 4.6 fJ/operation. Note that clock frequency is twice less than for DFF_{SET}, since it is triggered twice during the clock cycle.

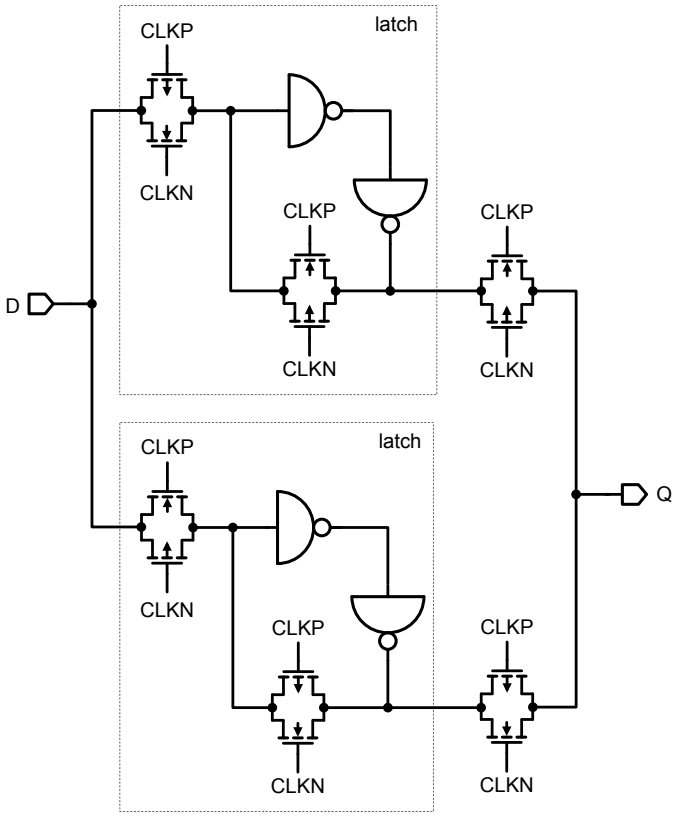


Figure 4.12: Dual edge triggered D-flip-flop circuit diagram

4.4.4 Dual Edge Triggered Sigma-Delta Modulator

First order modulator implemented with dual edge triggered flip flops described in previous section provides some benefit in energy consumption, but does not offer any improvement in occupied area – the number of full adders and flip-flops is the same as in the case of single edge triggered version. Moreover, dual edge triggered flip-flop has additional 4 transistors at the output. Another disadvantage of DET realization is a need of twice lower triggering frequency, i.e. $f_{ref}/2$. This results in additional divide-by-two element in a feedback path of a frequency divider.

Based on the concept of dual edge triggering, a modification to conventional implementation of the first order sigma-delta modulator (Fig. 4.7) with reduced transistor count is proposed. Proposed modulator is triggered by the reference frequency f_{ref}.

The underlying idea of the dual edge triggered first order modulator is as follows. Accumulating procedure is divided in two steps: at the first step least significant bits of the input signal A[n] are added to the value stored in accumulator, at the second step, using the result obtained after the least significant bit addition, most significant bits are accumulated. Both steps are performed using the same hardware. Fig. 4.13 illustrates the idea.

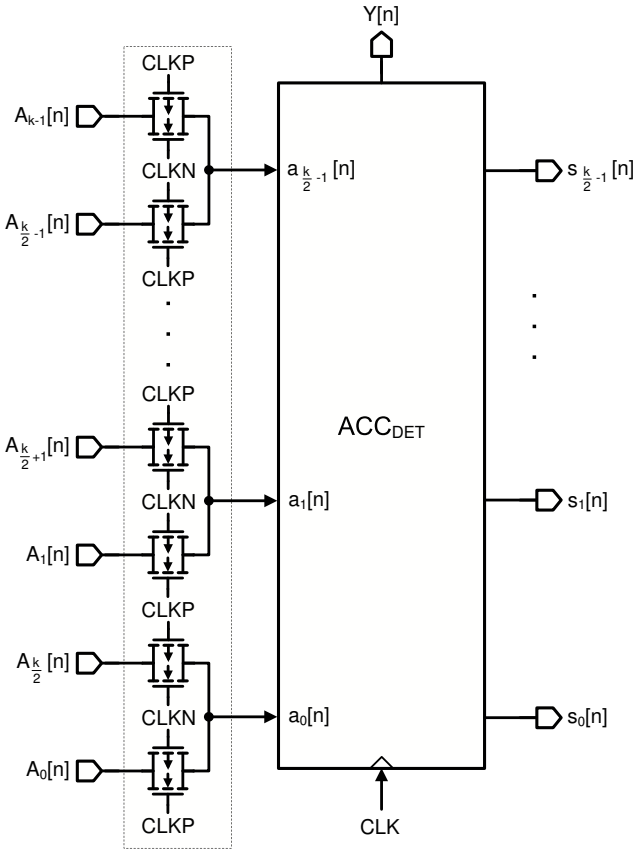


Figure 4.13: Dual edge triggered sigma-delta modulator

Input multiplexer applies least significant bits $A_0[n]...A_{k/2-1}[n]$ when CLKP = '1' and most significant bits $A_{k/2}[n]...A_{k-1}[n]$ when CLKP = '0' to the dual edge triggered accumulator ACC_{DET}. Note that accumulator has k/2 inputs. Internal structure of ACC_{DET} is presented in Fig. 4.14.

Full adder implementation, the same as mentioned above, is shown in Fig. 4.8. The number of FAs and D-flip-flops in the accumulator is k/2. In spite of the twice reduced count of 1-bit accumulating elements, still k bits of the information must be stored at each triggering step. Consequently, each flip-flop should be able to save 2 bits of information relating to the most and the least significant part of the accumulated word. Fig. 4.15 illustrates dual edge D-flip-flop implementing such a function. An important feature of such DFF_{DET} is that it captures the input value at previous edge of the clock signal and outputs the stored value at the next clocking edge. It consists of two single edge triggered flip-flops connected in parallel and combined by the multiplexer. The upper part of the DFF_{DET} is triggered by the rising edge of CLKP, the lower part – by falling. Output multiplexer is designed in such a way, that stored value in the upper flip-flop is routed to the output during the negative level of CLKP signal (transmission gate formed by transistors M_{n1} and M_{p1} is transparent) and stored value in the

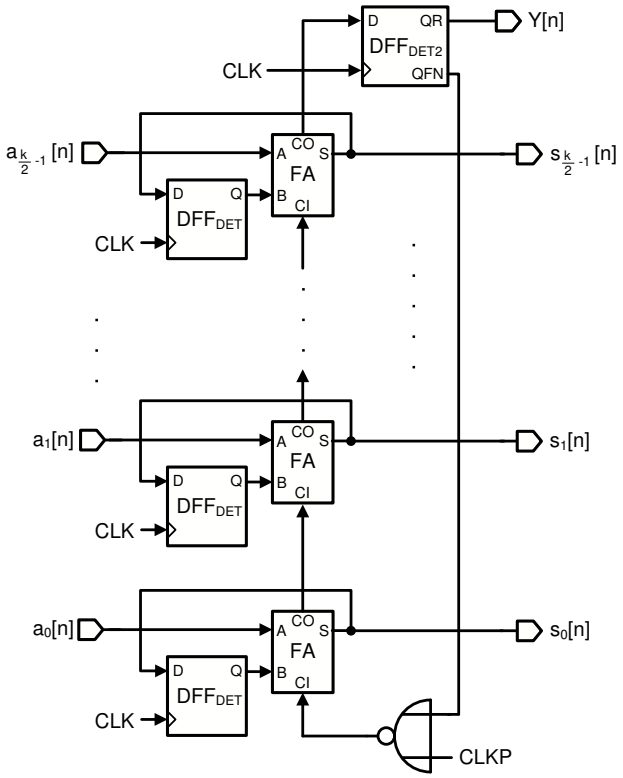


Figure 4.14: Block diagram of a dual edge triggered accumulator ACC_{DET}

lower flip-flop is routed to the output during the positive level of CLKP signal (transmission gate formed by transistors M_{n2} and M_{p2} is transparent). The timing diagram of DFF_{DET} is demonstrated in Fig. 4.16.

The last block unexposed by now is DFF_{DET2}. It consists of two single edge triggered D-flip-flops sharing one data input and having two outputs. It differs from DFF_{DET} in the absence of multiplexer at the output. The lower flip-flop triggered by the falling edge of the CLKP signal outputs inverted value of the stored signal. The circuit implementation of DFF_{DET2} is demonstrated in Fig. 4.17.

Returning now to Fig. 4.14, accumulator operates as follows. When the rising edge of CLKP arrives k/2 least significant bits of the input signal are applied to the accumulator. Since CLKP = '1' NOR gate (see Fig. 4.18 for realization details) which is placed in front of carry-in terminal of the first adder generates logical zero. Accumulator performs the addition of least significant bits. At the end of the first half of the clock period, carry out bit is ready at CO terminal of the last stage and is applied to the data input of DFF_{DET2}.

For performing the addition of the next half of the input word, carry-out bit obtained after the addition of the first half of the word is required. Thus, when the falling edge of CLKP appears, DFF_{DET2} outputs inverted carry-out bit of the last accumulating stage, which after inversion by NOR gate (now CLKP =

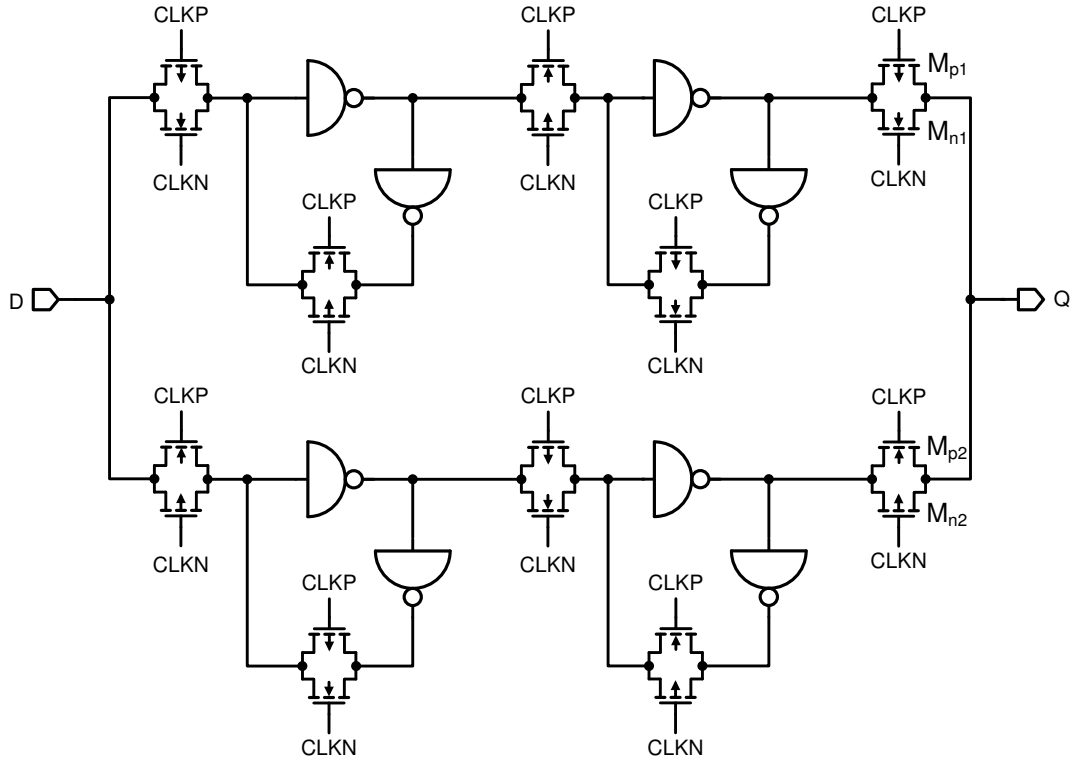


Figure 4.15: DFF_{DET} implementation

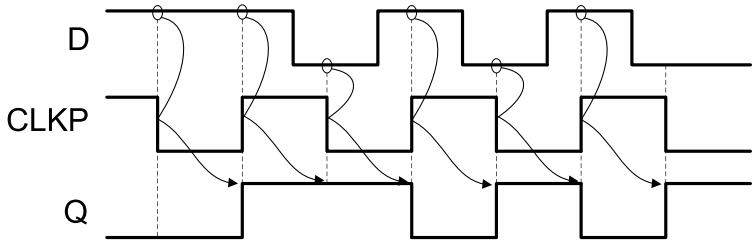


Figure 4.16: Timing diagram of DFF_{DET}

'0') goes to the carry-in terminal of the first stage. The addition of the most significant bits is performed. At the next rising edge, DFF_{DET2} outputs overflow bit, which is the output of the sigma-delta modulator.

An important observation: in dual edge triggered sigma-delta modulator accumulated value S[n] (which equals the quantization error with a negative sign, see (4.25)) changes twice during the clock period – at the high level of CLKP first half of the S[n] appears, and at the low level of CLKP another part of S[n] appears. This serves as a useful feature when first order modulators are cascaded in MASH structure because no additional interstage multiplexer is required.

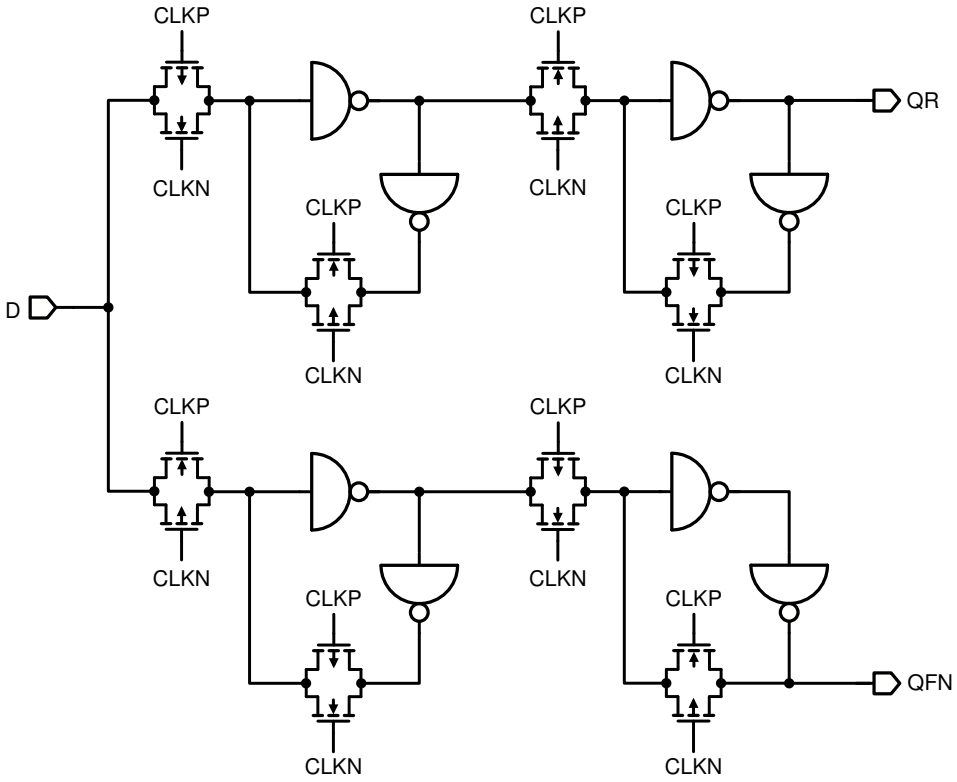


Figure 4.17: Implementation of DFF_{DET2} in Fig. 4.14

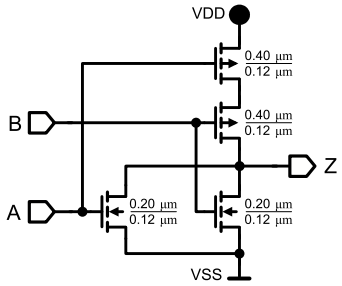


Figure 4.18: NOR gate implementation

Simulation Results

A set of simulations were carried out to evaluate performance of the proposed dual edge triggered first order sigma-delta modulator. A comparison with a conventional singe edge triggered counterpart is made. The following performance criteria are considered: energy consumption, switching characteristics resulting in a digital noise injection into the supply path, and device complexity showing the number of active elements or occupied area when implemented in an inte-

grated circuit.

DFF_{DET} is based on the single edge triggered flip-flop implementation: the sizes of all n-channel transistors are W/L = 0.2μm/0.12μm and p-channel transistors W/L = 0.4μm/0.12μm in all transmission gates and inverters. Due to the increased complexity, additional energy consumption is predicted. Time interval required for performing one operation is $1/f_{CLK} = 1/f_{ref}$. Increased data rate of the signal applied to the D terminal results in further growth of energy consumption. Simulation gives W_{op} = 13.6 fJ/operation. DFF_{DET2} consumes the same energy as DFF_{DET}.

In spite of the twice reduced number of full adders in the modulator, their switching activity is doubled: while in the single edge triggered accumulator they were changing state once in a clock period, in ACC_{DET} they are switching after both rising and falling edges of the triggering signal. Assuming the interval of one operation to be equal to clocking period, energy consumed by FA in dual edge triggered accumulator will be 34 fJ/operation, which is twice the value for FA in single edge triggered implementation.

Finally, knowing the power supply characteristics of each block, energy consumption of the whole sigma-delta modulator can be estimated. k-bit single edge triggered modulator (Fig. 4.7) consumes in the worst case $k \cdot (17 + 4.8) = 21.8k$ fJ/operation. Dual edge triggered modulator, ignoring DFF_{DET2}, NOR gate and input multiplexer, will consume $k/2 \cdot (13.6 + 34) = 23.8k$ fJ/operation, which is around 9% higher than a single edge triggered modulator.

As an example two 14-bit modulators were simulated. As a stimulus static digital signal was applied to both devices. Fig. 4.19 illustrates power supply network configuration. 0.3 nH inductance in series with 1 Ω resistance represent a single bondwire of roughly 0.3 mm long. 5 pF capacitor and 2 Ω resistor model an on-chip blocking capacitor for quietening the voltage at internal supply terminals. The model would be more correct if blocking capacitors were placed between VSS and VDD terminals, but such model provokes convergence problems during the transient simulation.

Simulation showed that DET modulator consumes 12% more energy than single edge triggered counterpart (312 fJ/operation versus 278 fJ/operation). A bit higer than predicted difference between two modulators is explaied by the presence of input multiplexer and some additional digital gates inside the DET, energy consumption of which was neglected. For higer resolution modulators energy difference will approach predicted value.

Next issue of interest is a switching supply noise of the modulators. As discussed in Section 3.2 pulsed behavior of supply current together with an inductive nature of a bond wire connection, results in the voltage spikes at VSS and VDD terminals of the circuit. The presented result of empirical analysis demonstrates the difference in a supply noise characteristics of DET and SET modulators. Simulation conditions are the same as in previous example – 14-bit modulators are

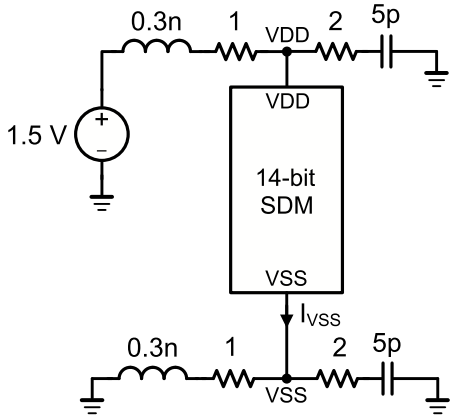


Figure 4.19: Simulation setup for estimating supply noise injection by single- and dual edge triggered modulators

connected as shown in Fig. 4.19; static input is used. Both circuits were simulated over the 200 ns time interval. The voltage at VSS terminal was observed in time and frequency domains. Fig. 4.20 demonstrates the result. DET modulator demonstrated lower peak values and peak deviation of the VSS voltage than SET circuit, however the difference is not significant. Fourier transformation of the VSS voltage exposes the difference invisible in time domain – the frequency component at f_{ref} is absent in dual edge triggered modulator; the amplitude of $2f_{ref}$ harmonic is almost the same for both SET and DET modulators.

In order to reveal the reason and explain such behavior of ground voltage change, the current I_{VSS} flowing through the ground terminal of the modulator is observed over the one clock cycle. The waveforms are shown in Fig. 4.21. All flip-flops in SET modulator are triggered by the rising edge of clock signal. This means that during some short interval immediately after CLKP goes high, all D-flip-flops are changing their output signal and all adders changing their state depending on the digital combination appeared at the input terminals. This cause current spikes within the time interval $t \in [t_{Ri}; t_{Fi}]$, see Fig. 4.21. The total amount of charge flowing through the VSS terminal after the rising edges of CLKP signal is

$$Q_{R.SET} = \sum_i \int_{t_{Ri}}^{t_{Fi}} I_{VSS.SET}(t)dt \tag{4.26}$$

Integration is performed over the time interval between rising and falling edges of CLKP signal.

Correspondingly, the charge flow caused by the falling edges is

$$Q_{F.SET} = \sum_i \int_{t_{Fi}}^{t_{Ri+1}} I_{VSS.SET}(t)dt \tag{4.27}$$

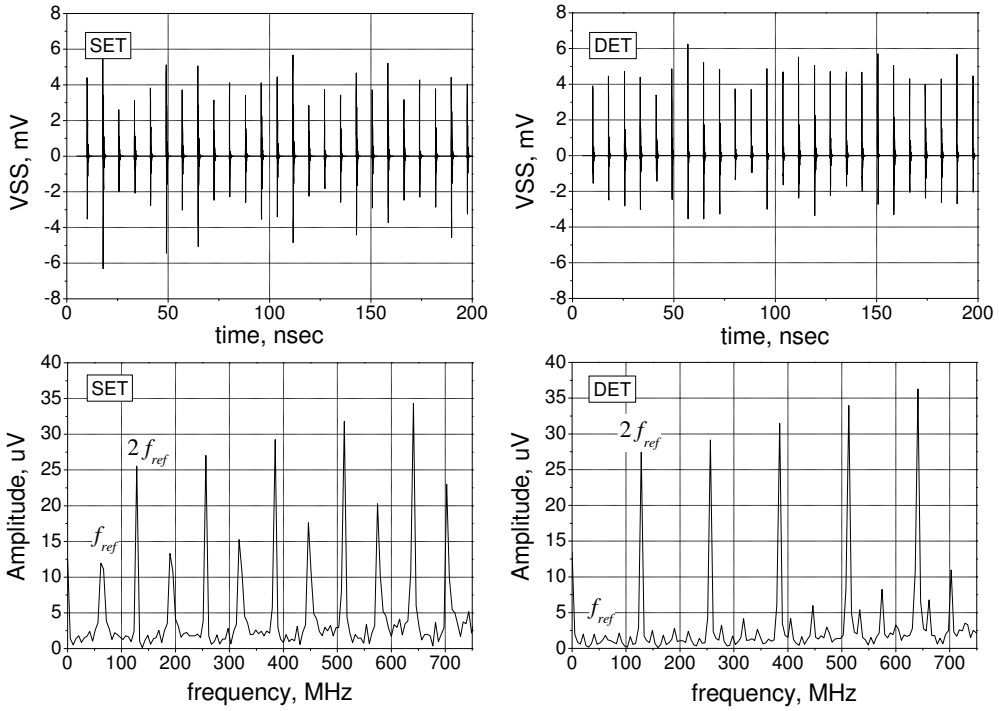


Figure 4.20: di/dt noise of 14-bit single- and dual edge triggered modulators in time and frequency domains; $f_{CLK} = f_{ref} = 64$ MHz

From Fig. 4.21 its clearly visible that

$$Q_{R.SET} > Q_{F.SET} \tag{4.28}$$

Equation (4.28) has unambiguous physical explanation: current flow during the falling CLKP edge is caused only by flip-flops changing their input state. Rising edge forces flip-flops, as well as adders, to consume the current. As a consequence of such supply current distribution, the period of $I_{VSS.SET}(t)$ waveform approaches $1/f_{ref}$, which results in a clear f_{ref} component at amplitude spectrum of $I_{VSS.SET}(t)$.

In contrast to SET modulator, DET implementation exhibits approximately equal charge flow at both rising and falling edges of triggering signal, namely

$$Q_{R.DET} \approx Q_{F.DET} \tag{4.29}$$

where

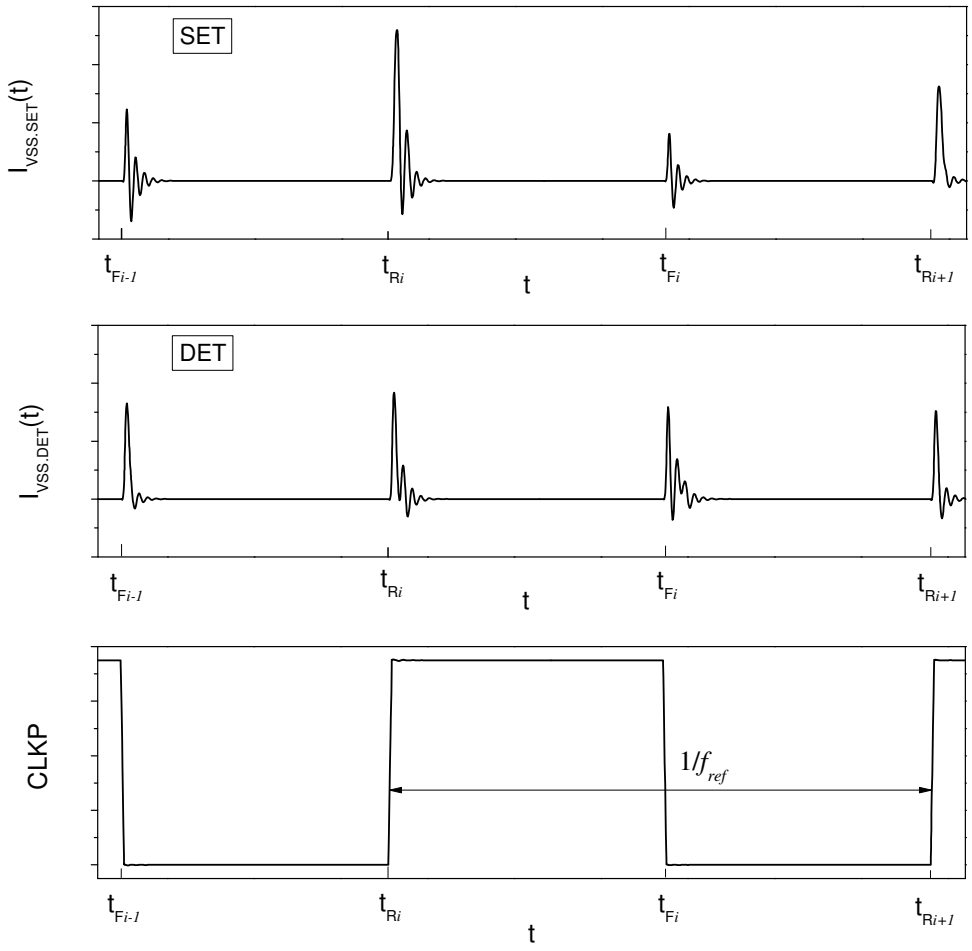


Figure 4.21: Current spikes generated at ground terminal of 14-bit single- and dual edge triggered modulators

$$Q_{R.DET} = \sum_i \int_{t_{Ri}}^{t_{Fi}} I_{VSS.DET}(t)dt \tag{4.30}$$

$$Q_{F.DET} = \sum_i \int_{t_{Fi}}^{t_{Ri+1}} I_{VSS.DET}(t)dt \tag{4.31}$$

The period of $I_{VSS.DET}(t)$ in DET modulator is close to $1/(2f_{ref})$, thus no significant component at f_{ref} in frequency spectrum is visible. In DET implementation all k/2 flip-flops and full adders are switching during both rising and falling edges of CLKP. Moreover, because of the reduced number of repetitive elements in the modulator, the total peak current is a bit lower.

The absence of f_{ref} component in amplitude spectrum of VSS voltage serves as a benefit when integrating in the shared substrate with analog PLL core. Every frequency component in substrate voltage perturbation is reflected in the PLL output signal as spurious tone. Elimination of first reference harmonic assures that first reference spur will not appear due to the switching action of sigma-delta modulator.

The last parameter falling in the focus of interest is modulators complexity. Single edge triggered modulator consists of k blocks, each including one 16-transistor D-flip-flop and one 28-transistor full adder, resulting in a total transistor count of $44k$. Dual edge triggered sigma-delta modulator comprises $k/2$ identical blocks with one 36-transistor DET flip-flop, 28-transistor full adder and 4-transistor input multiplexer. This gives $68(k/2) = 34k$ active elements. Furthermore, modulator includes additional DFF_{DET2} (32 transistors) and NOR gate (4 transistors), which results in $34k + 36$ transistor device. 14-bit DET features 18% less transistors than SET modulator.

4.5 MASH 1-1-1 Sigma-Delta Modulator

Multistage noise shaping (MASH) sigma-delta modulator proposed and implemented as an analog device in [Matsuya 87], was aimed to solve the problem of higher order modulator stability. The heart of a MASH structure is a low order (frequently used first order) modulator. The outputs of all stages are combined together by means of a linear network. The principal idea of the MASH modulator operation is the following: each stage obtains a quantization error of the preceding stage with a negative sign and performs its quantization; in the linear network quantization errors of all stages except the last one are canceled and only the high order shaped quantization error of the last stage remains in the output signal.

MASH 1-1-1 is referred as a third order multistage sigma-delta modulator containing three stages of the first order each. MASH 1-1-1 architecture is an attractive choice for using in monolithic frequency synthesizers because of its unconditional stability, ease of integration, and relatively highly decorrelated output sequence in the case when dithering is applied [Muer 02].

4.5.1 Linear Model

Fig. 4.22 shows the linear model of a MASH 1-1-1 modulator. Each first order stage is represented by an error feedback structure (see Section 4.4.3). Error feedback structure directly outputs the quantization error with a negative sign which is used as an input for the following first-order stage. Error compensation network is based on the adders and differentiators. Referring to the model,

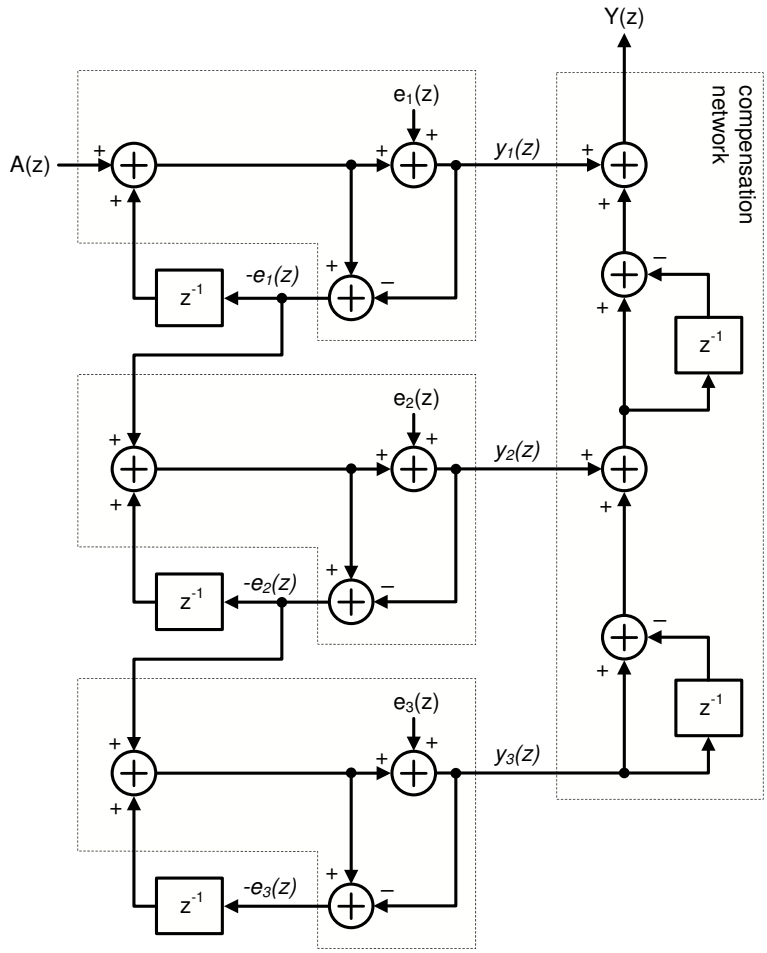


Figure 4.22: Linear model of a MASH 1-1-1 sigma-delta modulator

$$\begin{aligned} y_1(z) &= A(z) + \left(1 - z^{-1}\right) e_1(z) \\ y_2(z) &= -e_1(z) + \left(1 - z^{-1}\right) e_2(z) \\ y_2(z) &= -e_2(z) + \left(1 - z^{-1}\right) e_3(z) \end{aligned} \tag{4.32}$$

$$Y(z) = y_1(z) + y_2(z)\left(1 - z^{-1}\right) + y_3(z)\left(1 - z^{-1}\right)^2 \tag{4.33}$$

Substituting (4.32) into (4.33) yields

$$Y(z) = A(z) + \left(1 - z^{-1}\right)^3 e_3(z) \tag{4.34}$$

Noise transfer function of a MASH 1-1-1 modulator is

$$H_{NTF}(z) = \left(1 - z^{-1}\right)^3 \tag{4.35}$$

Mapping the NTF of MASH modulator into a power spectral density of a phase noise source in a linear model of a PLL gives:

$$\phi^2_{sdm}(f_m) = \frac{\pi^2}{3f_{ref}} \left(2 \sin\left(\frac{\pi f_m}{f_{ref}}\right)\right)^4 \tag{4.36}$$

The result is obtained by substituting (4.35) into (4.21).

If sigma-delta modulator controls feedback frequency divider (the most frequently used scheme), the noise introduced into the loop by modulator is low-pass filtered by the PLL transfer function. According to (4.36) MASH generates maximum noise at the offset which is half of the reference frequency, namely:

$$\phi^2_{sdm.max} = \phi^2_{sdm}(f_{ref}/2) = \frac{\pi^2}{3f_{ref}} \tag{4.37}$$

Sigma-delta modulator's noise can become dominating over the VCO noise at frequency offsets close to $f_{ref}/2$ if loop bandwidth is not sufficiently low to filter out high frequency modulator's noise. This places a limitation on the maximum value of the loop bandwidth. On the other hand, decrease of loop bandwidth leads to the higher phase noise at low frequency offsets. A tradeoff between the high-frequency phase noise overshoot caused by a high order modulator and increased in-band noise due to the low loop bandwidth is a bottleneck of a sigma-delta fractional-N synthesizer.

4.5.2 Tonal Performance

Fractional spurious tones in the sigma-delta PLL can appear because of the periodicity of modulator's signal or as a consequence of nonlinear distortion influence on modulator's sequence.

Multibit high order modulators are known to have better spurious performance than single-bit low order structures. For this reason MASH modulators, which are inherently multibit and high order, demonstrate good tonal performance by generating highly decorrelated sequences. PLL controlled by the undithered k-bit MASH 1-1-1 modulator will generate the best-case spurious at frequency offsets

$$f_{m.sp} = n \cdot (f_{ref}/2/2^k) \tag{4.38}$$

apart from the carrier, where f_{ref} is a reference frequency and $n \in N$ [Solomko 06]. The capacity of all stages equals k.

Similarly as it was already stated in (4.23) for a first order modulator, the best case spurious for MASH is demonstrated if the least significant bit of the first stage is set to the active level.

If the capacity k is relatively high, the fractional spurs will be so dense each to the other, that they could be treated as a phase noise. For example, in [Miller 91] sigma-delta PLL controlled by 24-bit MASH 1-1-1 modulator with active least significant bit generated insignificant fractional spurs. However, when the resolution is not that high, modulator can cause visible fractional spurs. For instance, fractional-N PLL controlled by the 10-bit MASH 1-1-1 modulator and triggered by the reference frequency of 64 MHz generates best case spurious at offsets $n \cdot 31.25$ kHz apart from the carrier [Solomko 06].

In [Chou 91] it was proved that digital MASH 1-1-1 modulator generates white quantization error if dithering is applied to the modulator. It is assumed that dither is a random, identically distributed process (which implies that its period approaches infinity) independent of modulator's input signal. This result applies to DC input signals.

A block diagram of a sigma-delta modulator with non-subtractive dithering is shown in Fig. 4.23. An output signal from the dither generator is added to the input signal and result is applied to the sigma-delta modulator. A dither is a digitally generated, usually identically distributed pseudo noise (PN) sequence. A PN generator implemented in hardware as a shift register with an XOR gate in a feedback loop (Fig. 4.24) generates a maximal length sequence of $2^n - 1$, where n is a shift register length [Mutagi 96]. Triggered by a clock signal with a reference frequency f_{ref}, the PN generator produces a dither with a period of $2^n / f_{ref}$. To achieve reasonable spurious suppression, capacity of a shift register must be relatively high. It's worth noting that Fig. 4.24 shows just the basic structure of a pseudo noise generator and it requires additional circuitry for detecting all-zero state. Indeed, if each flip-flop would have logical '0' at its output, the generator would be latched to this state. Additional circuitry for avoiding the zero state makes generator more complicated. In order to avoid noise degradation in the baseband, additional high-pass prefiltering of dithering sequence can be done. Alternatively, PN sequence can be added not at the input, but inside the sigma-delta modulator, where it will be filtered by the modulator itself [Norsworthy 92].

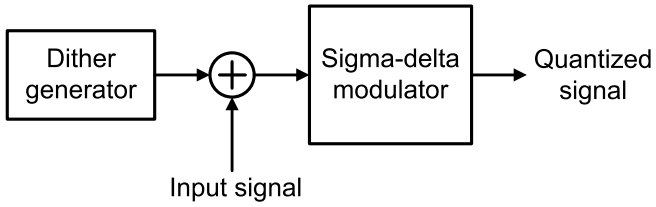


Figure 4.23: Dithered sigma-delta modulator

In [Norsworthy 92] it is advised to apply an independent dither to each stage of the MASH modulator. Dither is introduced either to the input of each stage or inside the stage to perform internal prefiltering. The merits of technique of separate dithering of each stage become apparent in analog multistage modulators, where

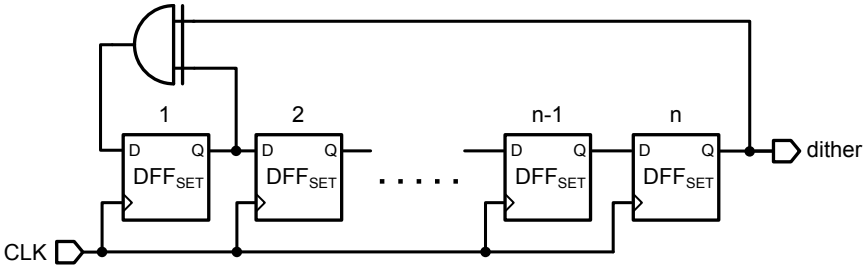


Figure 4.24: Hardware implementation of dither generator

dithering helps to smooth the tones which appear because of imperfect matching between stages. The use of separate dithering in digital multistage modulators might seem unnecessary because of the absence of nonlinear distortions in the digital device, however as one of the results of this work, the idea of applying dither to all stages was used for designing MASH 1-1-1 modulator with DC dithering. Section 4.7 describes the proposed implementation in details.

Fractional-N PLL controlled by the tone-free digital signal can generate powerful spurious at the output if some significant nonlinearities are presented in the system [Muer 02]. The use of analytical solution for spurious prediction caused by nonlinearities is possible only for simplest low order structures. Practically it is done by exhausted discrete-time simulations of a device for all possible input combinations. An experience obtained after the simulation of sigma-delta modulators for practical use showed that nonlinearly distorted modulator's sequence is mostly corrupted by spurious when the input word lies in the vicinity of upper and lower most values. In this case powerful spurious signals appear at low frequency offsets.

4.5.3 Hardware Implementation

Hardware implementation of MASH 1-1-1 modulator is shown in Fig. 4.25. The implementation is based on the first order sigma-delta modulators, namely, accumulators. In Fig. 4.25 accumulator is realized in a single edge-triggered style and its circuit diagram is shown in Fig. 4.7. The quantization error of each first order stage is applied to the input of the following stage.

Compensation network shown in Fig. 4.25 is based on differentiators and adders and generates a signed digital word Y[n] (the most significant bit is used as a negative/positive sign). A prescaler controlled by the sigma-delta modulator usually operates with unsigned numbers. Fig. 4.26 shows the diagram of a compensation network which converts internally its output signal from signed to unsigned form. The inverted overflow bit $y_1[n]$ of the first stage is subtracted from the output of the second differentiator. Inverted bit of the obtained result gives unsigned word Y[n].

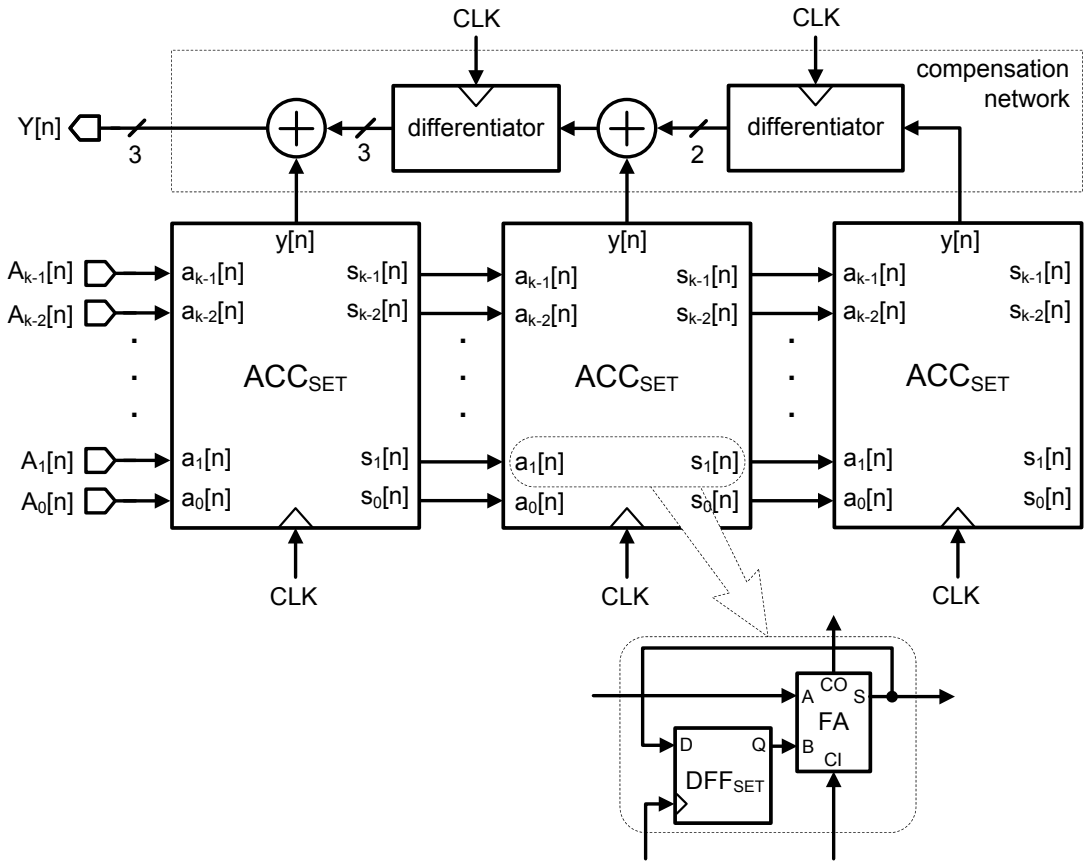


Figure 4.25: MASH 1-1-1 implementation

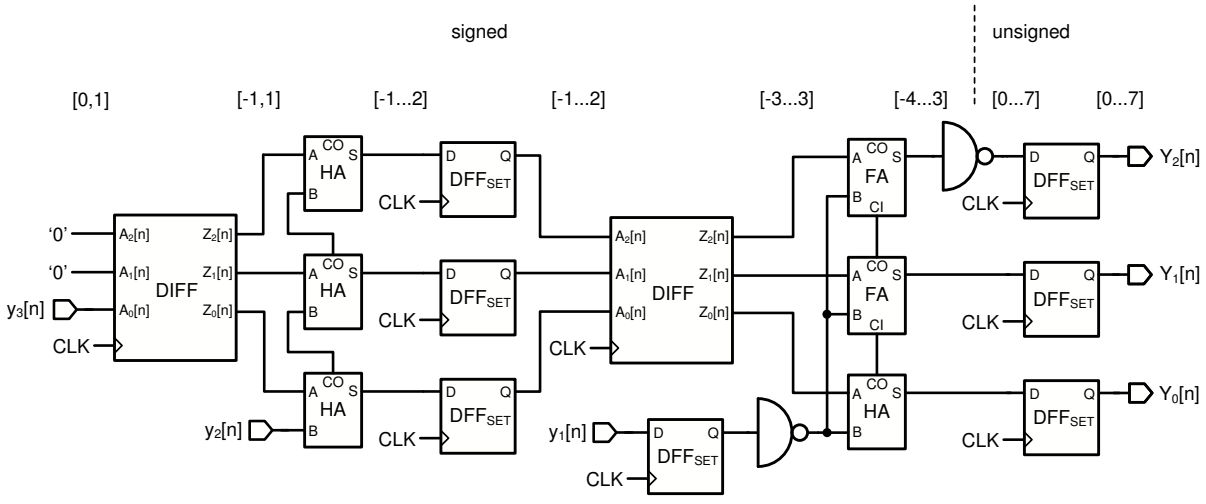


Figure 4.26: Compensation network with unsigned output

If the MASH 1-1-1 sigma-delta modulator with unsigned output controls a 8 modulus prescaler with the division ratios of $N, N+1, \ldots, N+7$, the fractional division ratio will be:

$$N_{frac} = N + 3 + A[n], \tag{4.39}$$

where $A[n] = (A_0[n] + A_1[n] \cdot 2 + \ldots + A_{k-1}[n] \cdot 2^{k-1})/2^k = const.$

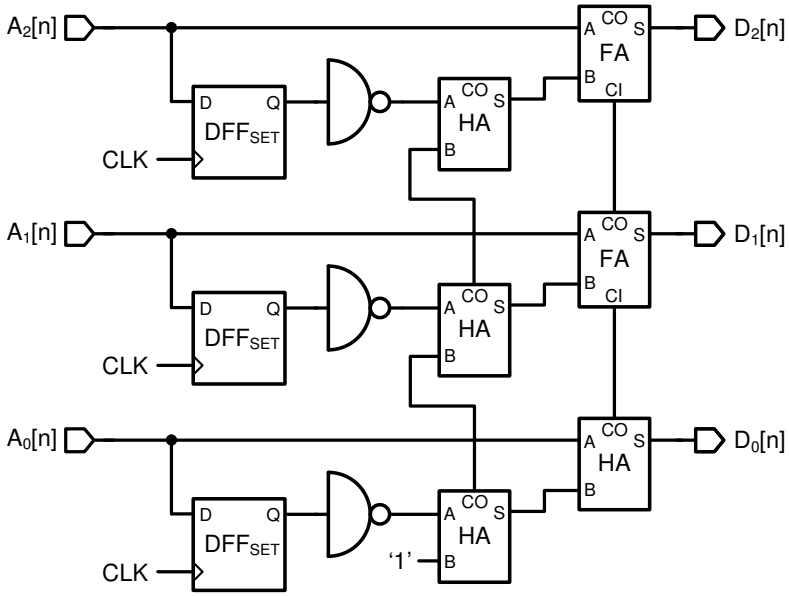


Figure 4.27: Differentiator (DIFF) implementation

Compensation network is pipelined by a register in front of the second differentiator and immediately after port y_1[n]. A register at the output of compensation network ensures that all bits of sigma-delta modulator's output Y[n] reach the frequency divider simultaneously.

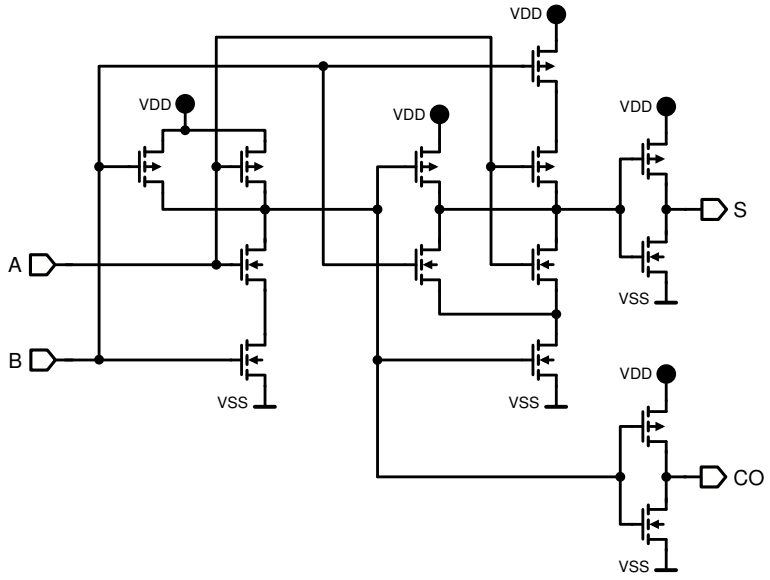
The logical diagram of a differentiator DIFF is presented in Fig. 4.27. It implements the following function:

$$D[n] = A[n] - A[n-1] \tag{4.40}$$

Subtraction is performed by inverting $A[n-1]$ and adding '1' to the result:

$$D[n] = A[n] - A[n-1] = A[n] + \overline{A[n-1]} + 1 \tag{4.41}$$

The circuit diagram of a half adder block used in compensation network is demonstrated in Fig. 4.28.



(a)

A	B	S	CO
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

(b)

Figure 4.28: (a) – half adder (HA) implementation, (b) – truth table of a half adder

4.5.4 Tonal Performance Simulation

As it was mentioned in Section 4.5.2, a dithered MASH 1-1-1 modulator generates white quantization error if dither is a non-periodic signal. However, pseudo-random dither generator commonly used in practical designs produces finite length sequence.

A set of simulations were carried out to verify the ability of pseudo random noise generators with different shift register length to smooth quantization noise spectrum of a modulator.

A logical model of a MASH 1-1-1 modulator is implemented in ADS environment. The model is assembled of primitive logical gates (D-flip-flops, AND, OR etc.) described in Verilog-A language. Verilog-A modeling offers much faster simulation than transistor level implementation, while providing accurate modeling of analog behavior of logical gates (such as supply current during the switching process and delay due to the finite input capacitances and output resistances). ADS also allows simulating mixed circuit-Verilog-A designs which makes possible efficiently predict the modulator's behavior with the presence of purely analog blocks (described by circuit-level models) in its structure.

The input resolution of the designed MASH 1-1-1 modulator is 14 bits (k=14). The least significant bit is used for applying a dither. The dither is generated by a pseudo-random noise generator demonstrated in Fig. 4.24 with different shift register length: 4, 8, and 13 bits. Static signal A[n] = 0.25 (corresponds to the

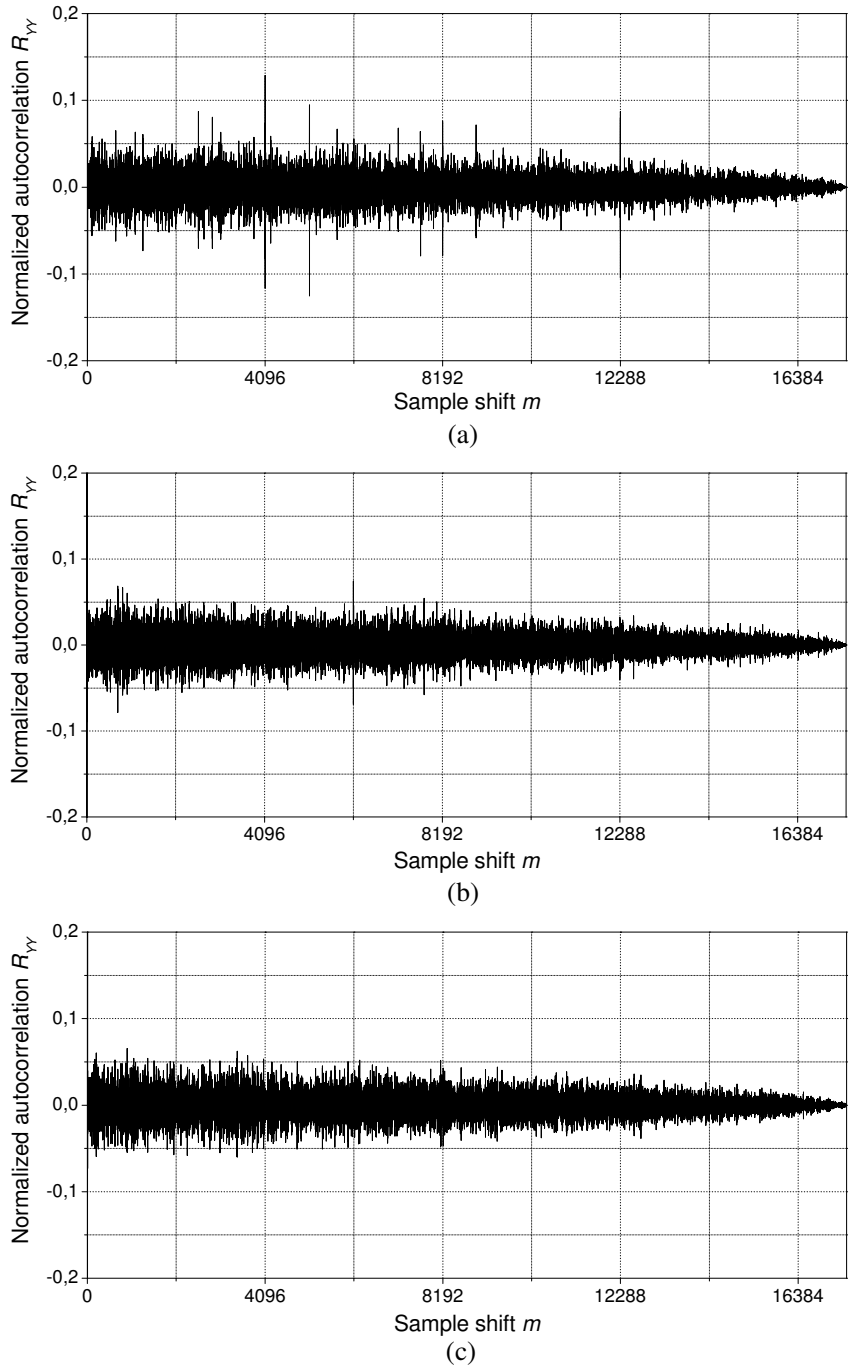


Figure 4.29: Discrete time autocorrelation estimate of the modulator output for the MASH 1-1-1 modulator with PN dither generator for different length of a shift register used in PN generator: (a) – 4 bits, (b) – 8 bits, (c) – 13 bits

binary representation A[n] = 0100000000000_2) is applied to the input. Such a fraction can place the worst case spur because least significant bits are inactive.

The length of generated output sequence Y[n] is N = 40000 samples. The output real values spread over the range of {–3, ..., 4} with the unity step.

The autocorrelation method is used for estimating periodicity of the generated sequence. It is preferable over the power spectrum method while it does not produce misleading results [Norsworthy 97].

The normalized discrete time autocorrelation estimate is given by [Norsworthy 97]:

$$R_{YY}[m] = \frac{1}{N}\sum_{i=1}^{N-m}(Y[i]-\overline{Y})(Y[i+m]-\overline{Y}), m \geq 0 \tag{4.42}$$

m is a sample shift, Y[n] is a decimal value of modulator's output. $\overline{Y}$ represents an average value of modulator's sequence Y[n] of length N:

$$\overline{Y} = \frac{1}{N}\sum_{i=1}^{N} Y[i], \tag{4.43}$$

and numerically equals the input word A.

Fig. 4.29 shows the obtained autocorrelation estimates of simulated sequences for different shift register length. The 4-bit dither generator is not able to smooth adequately the quantization noise of the MASH modulator, since spikes in Fig. 4.29(a) are clearly visible. 8-bit generator reduces the periodicity much more efficient. Spikes disappear totally only in the case when 13-bit dither generator is used. Based on the obtained results it might seem reasonable that at least 10-bit register is required to obtain sufficient spurious suppression for such modulator architecture and input resolution. Minimum 10 D-flip-flops and one XOR gate are required for implementing 10-bit shift register. However, in order to ensure that PN generator will not be latched into, for instance, all-zero state, additional logic is required. This sophisticates the circuit.

4.6 Dual Edge Triggered MASH 1-1-1 Modulator

Dual edge triggered implementation of MASH 1-1-1 modulator proposed in this work is based on the dual edge triggered sigma-delta modulator of the first order (see Section 4.4.4). The implementation changes neither architectural nor logical behavior of MASH 1-1-1 modulator. Both linear model analysis presented in Section 4.5.1 and formula (4.39) for average division ratio estimation hold true for dual edge triggered MASH modulator.

4.6.1 Motivation

Three first order stages in the MASH 1-1-1 modulator are the most considerable part of the device, which consumes up to 80% of the hardware. Switching noise performance of the whole modulator strongly depends on the switching noise characteristics of the first order stages.

As it was demonstrated in Section 4.4.4, dual edge triggered first order sigma-delta modulator distributes switching events in such a manner that the power is moved out of the odd multiplies of triggering (reference) frequency to the even multiplies of reference frequency.

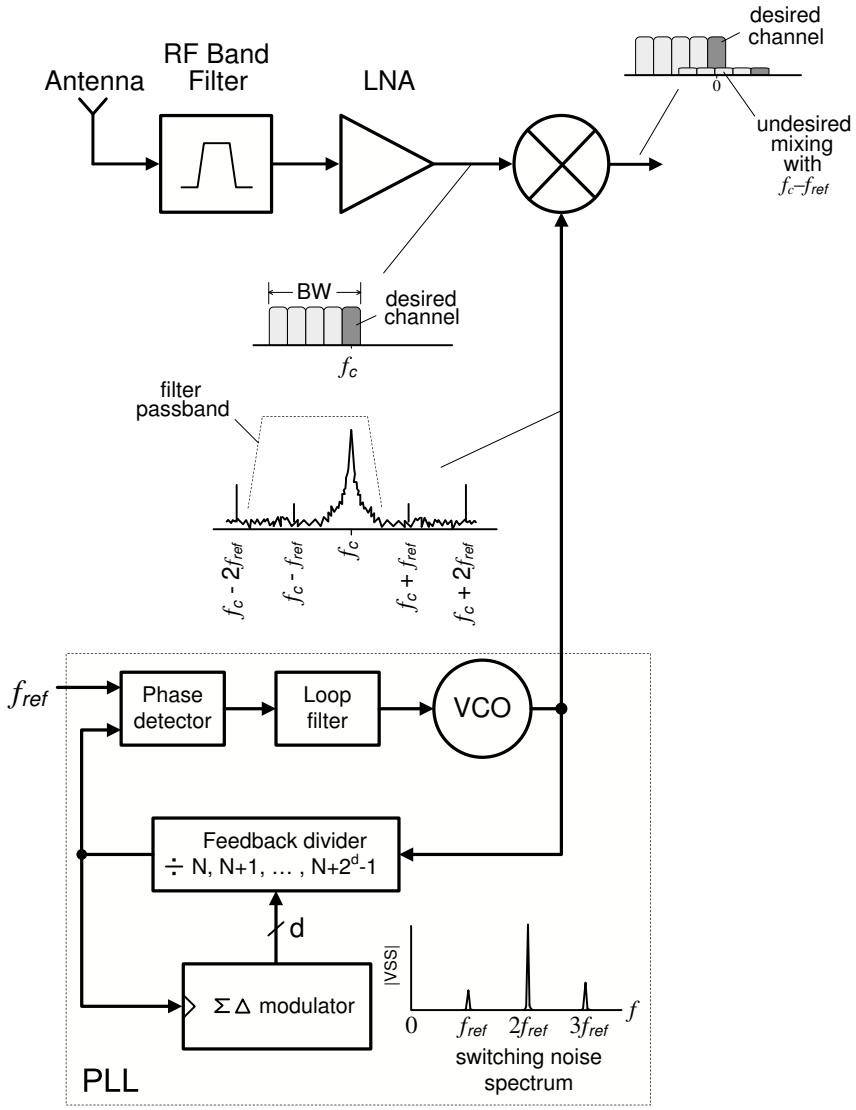


Figure 4.30: Receiver front-end

Distributed harmonics in switching noise spectrum will alter the power of refer-

ence spurs in high frequency PLL signal. In Section 3 in Fig. 3.1 the mechanism of supply noise tones to spurs mapping in an integrated sigma-delta synthesizer is shown. Digital switching noise of a sigma-delta modulator couples into the integrated VCO and loop filter through the common substrate. As a result, spurious tones at frequency offsets f_{ref}, $2f_{ref}$, $3f_{ref}$ and so on appear at the output of the synthesizer. The power of spurious tones depends on the amplitude and frequency of the corresponding harmonic in switching noise spectrum. Because dual edge triggered implementation offers much lower harmonic at f_{ref} as a conventional single edge triggered modulator, first reference spur in PLL output signal will be lower than the second one.

The benefit of such reference spurs distribution is twofold. Firstly, switching noise coupling is frequency dependent. For instance, noise coupled into the charge pump will be shaped by the loop filter. Since loop filter has a low-pass transfer function with a cutoff frequency not exceeding several megahertz, moving reference harmonic out by an octave will reduce the amount of noise coupled into the VCO. Even in spite of the fact that coupling path also contains reactive elements, switching noise can be partly suppressed by the loop filter when it is pushed to the higher frequencies. Only if the noise couples directly into the VCO coil, the higher frequency components can be transformed into the more powerful reference spurs.

In order to demonstrate the second benefit of reference spurs distribution, an integrated direct conversion receiver in Fig. 4.30 is considered. The receiver comprises an antenna, RF band filter, LNA, mixer and a sigma-delta PLL. Note that in Fig. 4.30 first reference spur is lower than the second one. In receiving path filter suppresses components outside the frequency range defined by the standard and required RF band is applied to the mixer. Together with a desired downconverted channel, interfering product caused by the mixing of first reference spur with undesired channel falls in the baseband. If reference frequency is chosen to be more than half of the RF bandwidth (BW), namely $\mathrm{BW} < 2f_{ref}$, no product caused by mixing with the second synthesizer spur falls into the baseband. Synthesizer which has lower first reference spur but higher second one is beneficial in such receiver, unless out of band blockers after LNA are more powerful than in-band signal (normally this does not happen).

With a proper choice of quartz frequency, second reference spur can be pushed out of the RF band specified by the standard, while the first one would have low power. An example of communication standard where such architecture can find a use is Bluetooth. The second sideband of a synthesizer synchronized by a 50 MHz crystal reference will be out of 80 MHz wide RF band of Bluetooth.

It might also seem reasonable to use reference frequency exceeding the RF bandwidth. However, high-overtone crystal oscillators (over 80 – 100 MHz) are usually more expensive and the power consumption of a sigma-delta PLL operating with high-frequency reference is higher.

Dual edge triggered modulator offers another advantage except switching noise

power distribution. Depending on the architecture and resolution proposed modulator occupies up to 20% less area than a conventional realization.

4.6.2 Hardware Implementation

The diagram in Fig. 4.31 demonstrates the implementation of the dual edge triggered MASH 1-1-1 modulator. The internal structure of ACC_{DET} is shown in Fig. 4.14 and the principles of operation are described in details in Section 4.4.4.

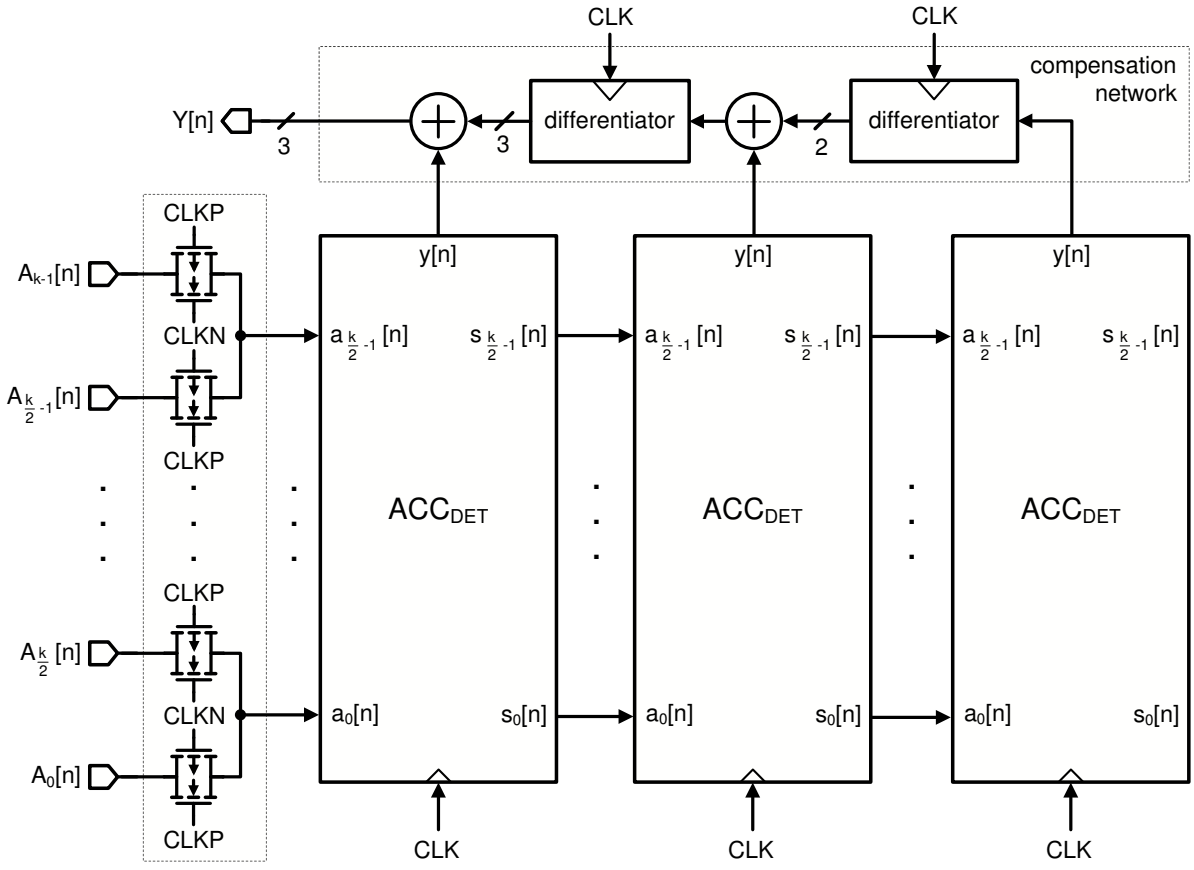


Figure 4.31: Dual edge triggered MASH 1-1-1 modulator implementation

The first stage consists of the dual edge triggered accumulator and multiplexer. The input multiplexer applies the least significant bits ($A_0[n]...A_{k/2-1}[n]$) when CLKP = '1' and most significant bits ($A_{k/2}...A_{k-1}$) when CLKP = '0' to the accumulator. During the least significant bits summation accumulator automatically outputs at $s_0[n]...s_{k/2-1}[n]$ least significant bits of the accumulated value. Correspondingly, during the most significant bits summation accumulator automatically outputs at $s_0[n]...s_{k/2-1}[n]$ most significant bits of the accumulated value. For this reason no multiplexer at the input of the second and third stages

is required. Each previous stage already performs a role of a multiplexer for the next stage.

For the reason of multiplexing, the DET implementation of MASH modulator will be more efficient if the number of bits in the input word A[n] is even.

All three stages generate overflow bit at the output y[n] once in a clock cycle, which is applied to the compensation network. The compensation network is realized in a conventional way, namely, single edge triggered style. Its block diagram is demonstrated in Fig. 4.26.

4.6.3 Simulation Results

14-bit input 3-bit output dual edge triggered MASH 1-1-1 modulator is designed in 0.13 μm CMOS technology. For performance comparison single edge triggered MASH 1-1-1 modulator with the same input and output resolution is designed.

The overall transistor count in the dual edge triggered modulator is reduced because of the full adders reuse. In order to implement three 14-bit accumulators in a conventional way 1896 transistors are required, while dual edge implementation needs 1486 transistors. 1-LSB dithering is applied to decorrelate the output sequence.

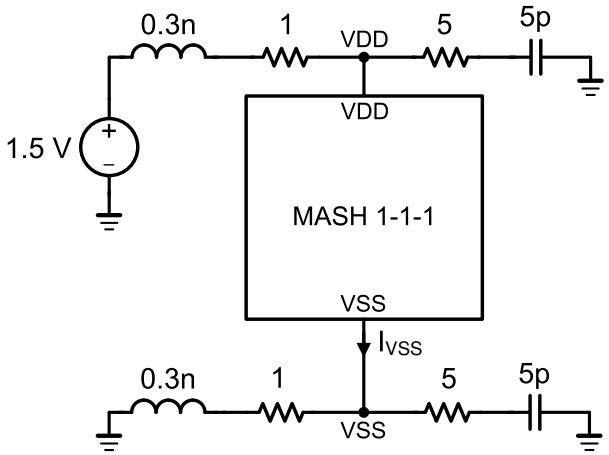


Figure 4.32: Simulation setup for estimating supply noise injection by single and dual edge triggered MASH 1-1-1 modulators

Simulation setup with the supply network scheme is presented in Fig. 4.32. Bondwires and supply buses inside the chip are modeled by 0.3 nH inductance and 1Ω resistance. Supply buses are blocked by 5 pF on-chip capacitors. In order to prevent convergence problems during the simulation, capacitors are connected between the supply nodes and ground, but not between VSS and VDD. 5Ω resistors damp the LC tank formed by the bond-wire inductance and blocking capacitors [Larsson 99].

As a stimulus for modulators static control signal with 1-LSB dithering is applied. Triggering frequency is $f_{ref} = 50$ MHz.

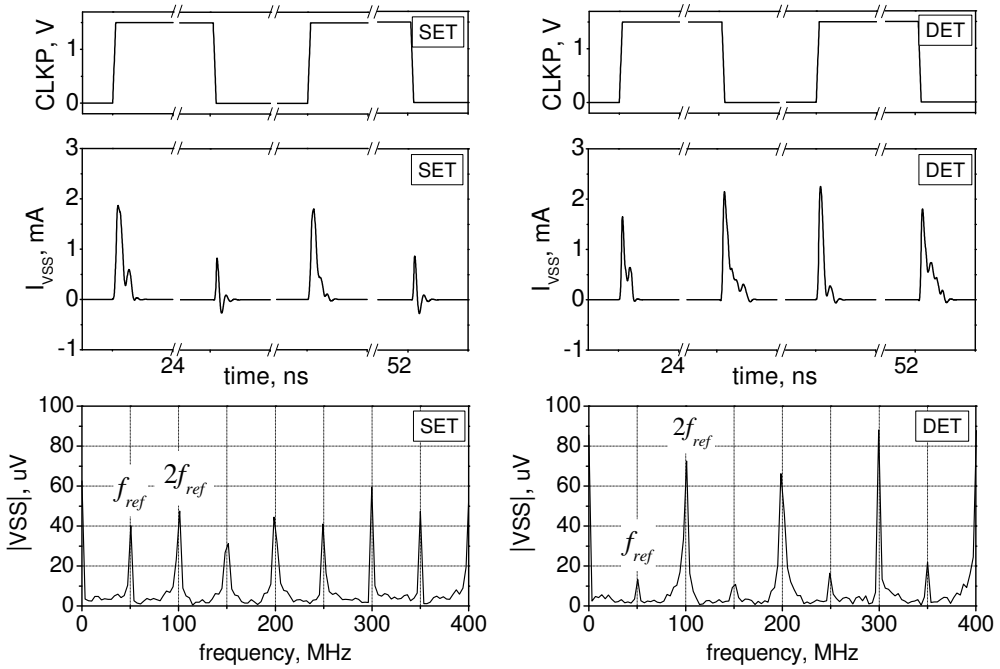


Figure 4.33: Switching noise of 14-bit single (SET) and dual (DET) edge triggered MASH 1-1-1 modulators in time and frequency domains

Fig. 4.33 demonstrates obtained waveforms of a supply current in time domain and amplitude spectrum of the substrate voltage VSS. In contrast to conventional MASH, both rising and falling edges in DET modulator exhibit similar amount of charge flow through the supply terminals, thus forcing the $\mathrm{I}_{VSS}(\mathrm{t})$ function to have the period close to $1/(2f_{ref})$. The first harmonic in amplitude spectrum of VSS voltage of dual edge triggered MASH is almost 4 times (12 dB) lower than the same harmonic in SET modulator (it is caused mainly by compensation network, which is implemented in a conventional way). The amplitude of the second harmonic is 1.5 times (3.5 dB) higher. Because of such charge distribution over the time, all odd harmonics in DET modulator are lower and even harmonics are higher than in SET implementation. Odd harmonics can be reduced further if compensation network would also comprise dual edge triggered flip-flops.

Simulation demonstrated very weak dependence of modulator's switching activity and, thus, supply current spikes level on the stimulus value in the case when dithering is applied.

4.6.4 Spurious Performance of a PLL with Dual Edge Triggered Modulator

The following analysis is performed to verify the PLL spurious performance improvement achieved with the dual edge triggered MASH 1-1-1 modulator. For this purpose a simple PLL model is used. Despite the distributed nature of switching noise source (sigma-delta modulator) and coupling paths they are presented by the lumped elements. Such representation is sufficient for estimating the difference in reference spurs power of PLL operating with single- and dual edge triggered modulators.

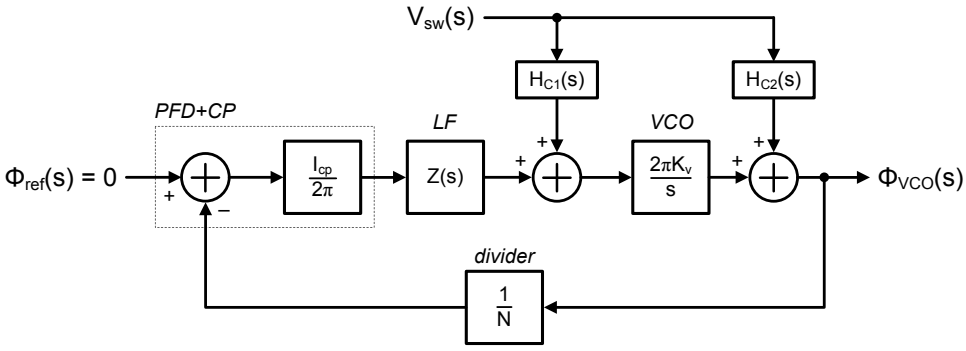


Figure 4.34: PLL linear model with introduced switching noise

Fig. 4.34 shows the PLL linear model into which the coupled switching noise of a sigma-delta modulator is introduced. Frequency domain source $V_{sw}(s)$ represents the switching noise of a modulator induced into the PLL by means of substrate coupling. In the model it is assumed that the noise couples mainly into the loop filter and the VCO. Before coupling into the PLL the noise is shaped by the transfer functions of the coupling paths $H_{C1}(s)$ and $H_{C2}(s)$. These transfer functions also take into account the location of noise injection in the analog block. For instance, the transfer function for noise introduced into the VCO depends on whether it couples into the integrated coil or active part of the oscillator.

The phase deviation at the output of the VCO:

$$\Phi_{VCO}(s) = H_L(s)\left(H_{C2}(s) + H_{C1}(s)\frac{2\pi K_v}{s}\right)V_{sw}(s) \tag{4.44}$$

where $H_L(s)$ is a high-pass PLL transfer function defined as

$$H_L(s) = \frac{s}{s + Z(s)I_{cp}K_v/N} \tag{4.45}$$

At frequency of reference signal $H_L(s) \approx 1$, thus (4.44) simplifies to

$$\Phi_{VCO}(s) = \left(H_{C2}(s) + H_{C1}(s)\frac{2\pi K_v}{s} \right) V_{sw}(s) = H_{LC}(s)V_{sw}(s) \tag{4.46}$$

Transforming phase deviation into the spurious tones at the output of PLL expressed in dBc [Vaucher 02], we obtain:

$$\begin{aligned} P_{sp}(\Delta f) &= 20\log\left(\frac{|H_{LC}(j2\pi\Delta f)V_{sw}(j2\pi\Delta f)|}{2}\right) = \\ &= 20\log\left(\frac{|H_{LC}(j2\pi\Delta f)|}{2}\right) + 20\log\left(|V_{sw}(j2\pi\Delta f)|\right) \end{aligned} \tag{4.47}$$

The estimation of absolute value of $P_{sp}(\Delta f)$ is a very complicated task because of the distributed nature of coupling path. The functions $\mathrm{H}_{C1}(\mathrm{s})$ and $\mathrm{H}_{C2}(\mathrm{s})$ are very layout dependent, especially for technologies with lightly doped non-epi substrates. However, the difference in spurious power for PLL with single- and dual edge triggered MASH modulators can easily be estimated. Assuming the independence of $\mathrm{H}_{LC}(\mathrm{s})$ on the noise source (such assumption seems reasonable if modulators occupy more or less similar area and layed out in a similar style), the spurious power difference defines as:

$$\begin{aligned} \Delta P_{sp}(\Delta f) &= P_{sp.DET}(\Delta f) - P_{sp.SET}(\Delta f) = \\ &= 20\log\left(\left|\frac{V_{sw.DET}(j2\pi\Delta f)}{V_{sw.SET}(j2\pi\Delta f)}\right|\right) \end{aligned} \tag{4.48}$$

where $P_{sp.DET}(\Delta f)$ and $P_{sp.SET}(\Delta f)$ are PLL spurs power with dual- and single edge triggered modulators respectively, $V_{sw.DET}(s)$ and $V_{sw.SET}(s)$ represent the switching noise introduced by the dual- and single edge triggered modulators.

Having the transistor implementation of the modulator and knowing the configuration of supply network, numerical values for $V_{sw.DET}(s)$ and $V_{sw.SET}(s)$ can be obtained by means of simulation. Estimated switching noise at VSS terminal of single- and dual edge triggered MASH 1-1-1 modulators is shown in Fig. 4.33. Similar amplitude spectrum is observed at VDD node. The numerical value of $\left|\frac{V_{sw.DET}(s)}{V_{sw.SET}(s)}\right|$ at f_{ref} and $2f_{ref}$ is taken from the diagrams:

$$\begin{aligned} \left|\frac{V_{sw.DET}(j2\pi f_{ref})}{V_{sw.SET}(j2\pi f_{ref})}\right| &= \left|\frac{VSS_{DET}(f_{ref})}{VSS_{SET}(f_{ref})}\right| = \frac{12\ \mu V}{40\ \mu V} = 0.3 \\ \left|\frac{V_{sw.DET}(j2\pi\cdot 2f_{ref})}{V_{sw.SET}(j2\pi\cdot 2f_{ref})}\right| &= \left|\frac{VSS_{DET}(2f_{ref})}{VSS_{SET}(2f_{ref})}\right| = \frac{73\ \mu V}{48\ \mu V} = 1.52 \end{aligned} \tag{4.49}$$

Substituting (4.49) into (4.48) gives:

$$\begin{aligned} \Delta P_{sp}(f_{ref}) &= -10.46\ dB \\ \Delta P_{sp}(2f_{ref}) &= 3.64\ dB \end{aligned} \tag{4.50}$$

Thus, if reference spurs are caused mainly by switching noise of the sigma-delta modulator, the use of dual edge triggered MASH 1-1-1 structure allows to decrease

the first reference spur by 10.46 dB while increasing the second one by 3.64 dB. Note that such result is valid only for the specific implementation of MASH modulator presented in Section 4.6.3.

4.7 MASH 1-1-1 Modulator with DC Dither in All Stages

A widespread dithering implementation in digital MASH modulators is setting the LSB of the input word into active level [Miller 91]. The density and power of fractional spurs in such a case is proportional to the capacity and order of the modulators compound stages. Equation (4.38) shows the dependence of fractional spurs density on the MASH 1-1-1 capacity. Significant capacity extension allows considerably compensate fractional spurs, but leads to an increase of the modulators complexity and size.

Based on the topology presented in [Norsworthy 92] the use of static dithering applied to all stages of MASH modulator is proposed [Solomko 06]. In contrast to [Norsworthy 92], in proposed topology dithering is applied directly to the input of each stage of the modulator. Modulator is implemented by means of adding extra bits to the second and third accumulators at which logical '1' is applied. Such simple modification to the conventional MASH structure offers the following merits:

1. It allows the reduction of the capacity of the first and second stages, while keeping dependence of spurious signals distribution only on the last stage;
2. Since constant logical '1' level is used as a dither, no additional circuit for dithering signal generation is required.

The two advantages mentioned above lead to decrease in modulator size and complexity and minimization of its influence on the analog part in the case of a fully integrated synthesizer. In spite of the improved periodicity of limit cycles, the described modulator still generates spurious tones since there is no randomness in the proposed device.

The proposed modification for spurious compensation concerns only nonlinear behavior of the modulator and leaves the quantization noise distribution without any change. This is proved by the computations using linear model of the modulator.

4.7.1 Linear Model

The linear model of a MASH 1-1-1 modulator with DC dither is presented in Fig. 4.35.

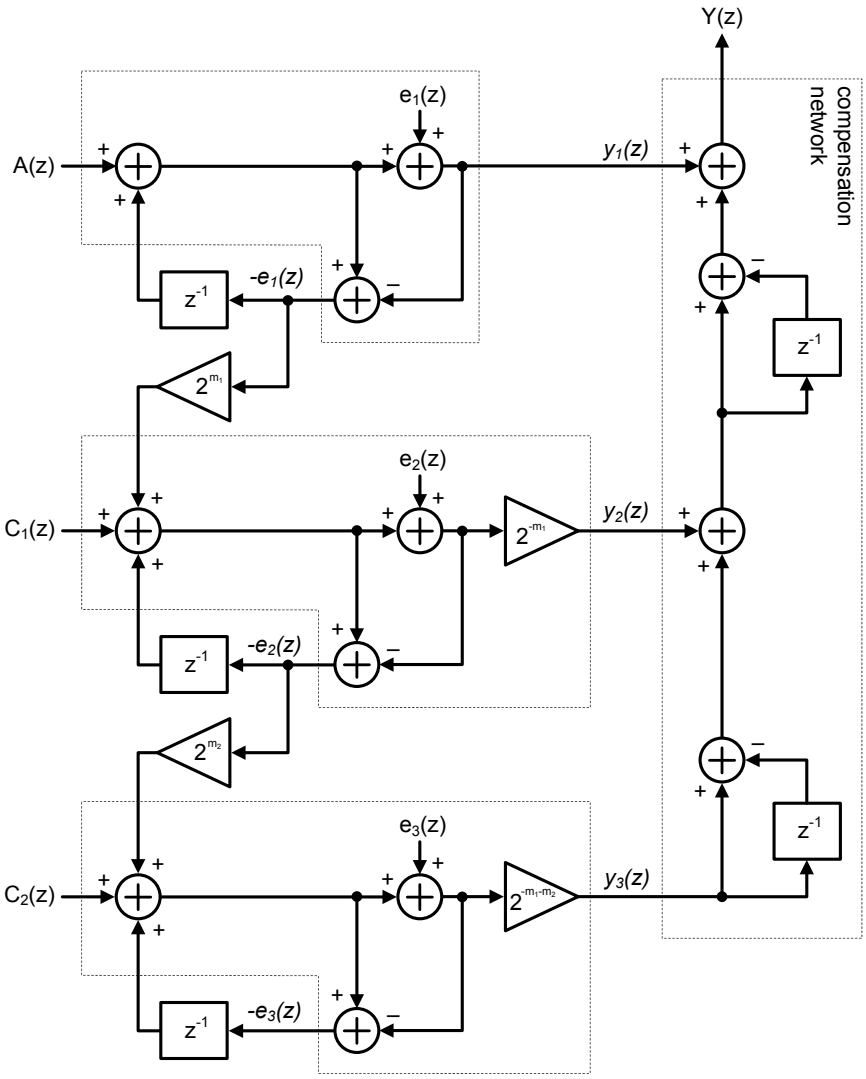


Figure 4.35: Linear model of a MASH 1-1-1 modulator with DC dither in all stages

The range of the input signal of the third stage is 2^{m_1} times higher than of the second stage and $2^{m_1+m_2}$ times higher than of the first stage. Quantization error of the first stage is multiplied by 2^{m_1} and is applied to the second stage. Additionally, dithering signal $C_1(z)$ is added to the input of the second stage. In the same fashion quantization error of the second stage is multiplied by $2^{m_1+m_2}$ and applied to the third stage together with the dithering signal $C_2(z)$. Both $C_1(z)$ and $C_2(z)$ are DC signals.

The following calculations present the output signal content for the model shown in Fig. 4.35.

$$y_1(z) = A(z) + e_1(z)(1 - z^{-1}) \tag{4.51}$$

$$y_2(z) = -e_1(z) + 2^{-m_1}C_1(z) + 2^{-m_1}e_2(z)(1 - z^{-1}) \tag{4.52}$$

$$y_3(z) = -2^{-m_1}e_2(z) + 2^{-m_1-m_2}C_2(z) + 2^{-m_1-m_2}e_3(z)(1 - z^{-1}) \tag{4.53}$$

$$Y(z) = y_1(z) + y_2(z)(1 - z^{-1}) + y_3(z)(1 - z^{-1})^2 \tag{4.54}$$

After substitution of (4.51), (4.52), and (4.53) into (4.54) and rearranging we obtain:

$$\begin{aligned} Y(z) = \quad & F(z) + 2^{-m_1-m_2}e_3(z)(1 - z^{-1})^3 + \\ & + 2^{-m_1-m_2}C_1(z)(1 - z^{-1})^2 + \\ & + 2^{m_1}C_2(z)(1 - z^{-1}) \end{aligned} \tag{4.55}$$

Since compensation signals $C_1(z)$ and $C_2(z)$ are DC signals, namely

$$\begin{aligned} C_1(e^{j2\pi f/f_{ref}})\big|_{f\neq 0} = 0 \\ C_2(e^{j2\pi f/f_{ref}})\big|_{f\neq 0} = 0 \end{aligned} \tag{4.56}$$

which are applied to the differentiator, which transfer characteristic equals zero at DC

$$(1 - z^{-1})\big|_{z=e^{j2\pi f/f_{ref}}, f=0} = 0 \tag{4.57}$$

then

$$\begin{aligned} 2^{-m_1-m_2}C_1(z)(1 - z^{-1})^2\big|_{z=e^{j2\pi f/f_{ref}}} = 0 \\ 2^{-m_1}C_2(z)(1 - z^{-1})\big|_{z=e^{j2\pi f/f_{ref}}} = 0 \end{aligned} \tag{4.58}$$

Finally, (4.55) simplifies to

$$Y(z) = F(z) + 2^{-m_1-m_2}e_3(z)(1 - z^{-1})^3 \tag{4.59}$$

Since in the first order modulator quantizer range matches the range of the input signal, the allowed range of an error $e_3(z)$ is $2^{m_1+m_2}$ times higher than $e_1(z)$. This means that the quantization error power distribution is the same as in conventional MASH 1-1-1 structure with accumulators of the same capacity.

The obtained equation (4.59) shows that there is no dependence of the output signal on the dither $C_1(z)$ and $C_2(z)$: it changes neither output DC component nor linear quantization noise distribution. Moreover, since $C_1(z)$ and $C_2(z)$ are static signals no high-pass prefiltering is required.

4.7.2 Hardware Implementation

The implementation of a three-stage MASH sigma-delta modulator with DC dither in all stages is based on the conventional MASH 1-1-1 modulator. For the ease of realization, quantization error multiply coefficients are the power of 2. This results only in additional bits added to the second and third stages. The capacity of the second stage is m_1 bits higher than the first stage. Correspondingly, last stage has $m_1 + m_2$ more bits than the first one.

Hardware realization shown in Fig. 4.36 implements the MASH 1-1-1 sigma-delta modulator with DC dither in all stages.

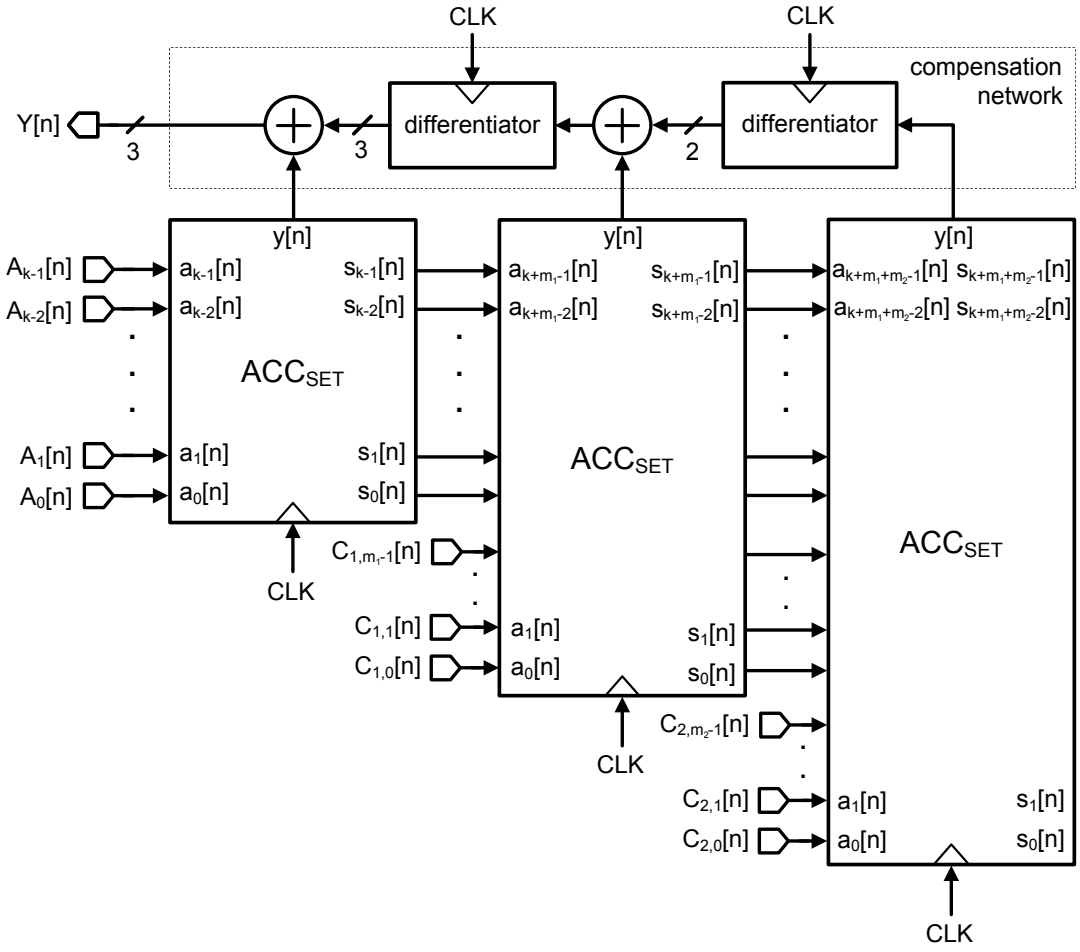


Figure 4.36: Implementation of a MASH 1-1-1 modulator with DC dither in all stages

The number and the power of spurious tones in sigma-delta modulator depends on the resolution and input signal applied to it. The input signal for the second and third stages changes from cycle to cycle, thus, spur density cannot be easily predicted knowing just the resolution of the accumulator.

According to (4.23), the second and the third stages will be the most efficiently dithered when the least significant bit of both dither signals equals '1', namely $C_{1,0}[n] =' 1'$ and $C_{2,0}[n] =' 1'$.

After adding the dithering signal to the subsequent accumulators, spurs move to the lower frequency offsets and their power decreases, yielding the spurious at frequency offsets

$$f_{m.sp} = n \cdot (f_{ref}/2^{k_3}) \tag{4.60}$$

where

$$k_3 = k + m_1 + m_2 \tag{4.61}$$

is the capacity of the last stage of MASH modulator.

4.7.3 Simulation Results

To verify practically the dithering capabilities of the presented topology a discrete time model of the MASH 1-1-1 modulator with DC dither in all stages was built in Matlab Simulink environment. The capacity of the first stage as well as the resolution of an input signal was chosen to be 10 bits. Each following stage is enhanced by 2 bits, resulting in a 12-bit second stage and 14-bit third stage. Referring to Fig. 4.36:

$$k \ = \ 10, \ m_1 \ = \ 2, \ m_2 \ = \ 2 \tag{4.62}$$

The simulation is performed for different input settings. The autocorrelation estimate is calculated for each obtained sigma-delta modulator's sequence. The sequence length in all cases is 50000 samples.

The best case tonal performance will probably be demonstrated in the case when logical '1' signal is applied to additional dithering bits of the second and third stages, namely $C_{1,0}[n] = C_{1,1}[n] = C_{2,0}[n] = C_{2,1}[n] = 1$, and the least significant bit of the input word is active: $A_0[n] = 1$. The obtained autocorrelation estimate for such input settings is demonstrated in Fig. 4.37. The exact value of the input signal was chosen to be 0.3134765625 which corresponds to the following binary representation: $A[n] = 0101000001_2$.

The most powerful peak of autocorrelation estimate is observed when the sequence is shifted by 16382 samples, or equivalently, 2^{k3}, where $k_3 = k + m_1 + m_2 = 14$. Thus, the output sequence repeats with a period 2^{k3} times exceeding the period of a sampling signal, exactly as predicted by (4.60). Another three peaks, appeared due to the higher rate periodicity, are much less powerful.

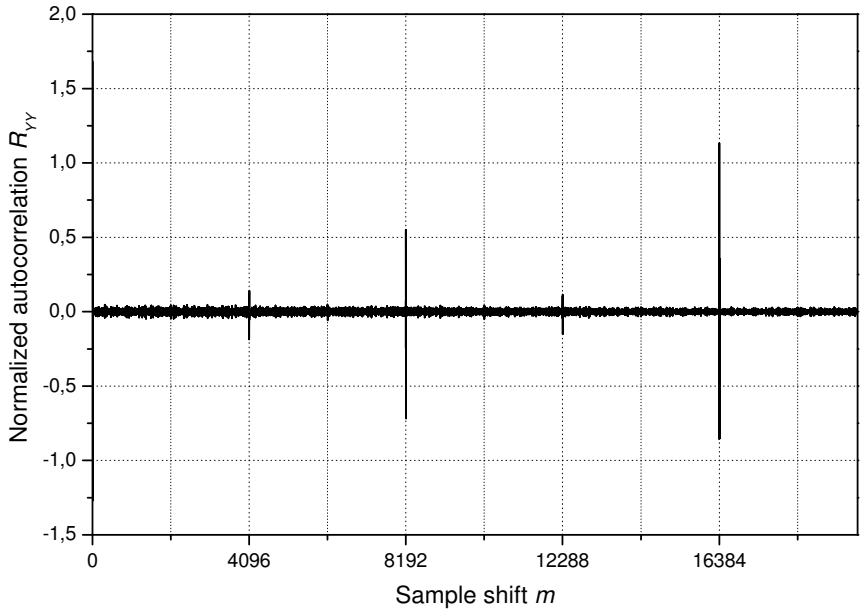


Figure 4.37: Discrete time autocorrelation estimate of the modulator output for the MASH 1-1-1 modulator with DC dither in all stages; $A[n] = 0101000001_2$, $C_{1,0}[n] = C_{1,1}[n] = C_{2,0}[n] = C_{2,1}[n] = 1$

For comparison, the discrete time autocorrelation estimate was calculated for the output sequences of the same modulator when no DC dithering is applied i.e. $C_{1,0}[n] = C_{1,1}[n] = C_{2,0}[n] = C_{2,1}[n] = 0$ and when least significant bit of the input signal equals zero and DC dithering is applied. The results are shown in Fig. 4.38 and Fig. 4.39 respectively.

Undithered modulator acts like a conventional MASH structure – the sequence repeats each 2048 samples giving the lowest frequency tone at $f_{ref}/(2 \cdot 2^k)$, where $k = 10$, f_{ref} is a sampling frequency (see Fig. 4.38).

In the case when dithering is applied, the result almost independent on the DC value applied to the input. The autocorrelation estimate for the worst-case input signal (least significant bits are zero) demonstrates almost the same peak distribution as in the best-case input signal – Fig. 4.39 shows the result. The highest spike appears at sample shift of 16384 and its power is the same as in Fig. 4.37.

Simulations performed with different values of input signal demonstrated weak dependence of the tonal performance on the DC value applied to the input in the case when DC dither to the second and third stages is applied.

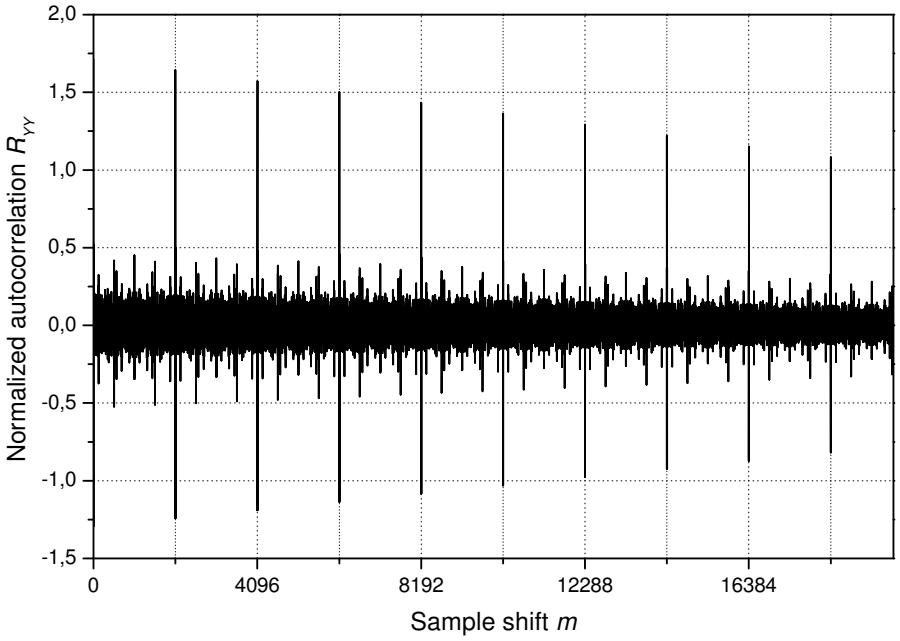


Figure 4.38: Autocorrelation estimate for the MASH 1-1-1 with DC dither in all stages; $A[n] = 0101000001_2$, $C_{1,0}[n] = C_{1,1}[n] = C_{2,0}[n] = C_{2,1}[n] = 0$

4.8 MASH 1-1-1 Modulator with Direct Feedback Dithering

The concept of hardware efficient implementation of digital sigma-delta modulators is materialized in MASH 1-1-1 modulator with direct feedback dithering. In this topology, as demonstrated in Fig. 4.40, the output signal of the compensation network is fed back directly to the input of the MASH modulator. For the simplicity, three least significant bits of the first stage are used for the dither and to the rest bits the control word A[n] is applied. Unfortunately, the dynamic range cannot be extended by adding the dither to A[n], since dither spreads over all 8 levels of 3-bit signal.

The output signal Y[n] can serve as a dither because it is always busy, unless zero is applied to the input of the modulator. Even in spite of the fact that Y[n] is correlated with A[n] because digital MASH 1-1-1 modulator is a finite state machine, such dither topology can still be efficient in smoothing quantization noise spectrum of the modulator.

Direct feedback dithering offers one advantage: since the output signal performs a role of a dither, no additional hardware for whitening the quantization noise is required.

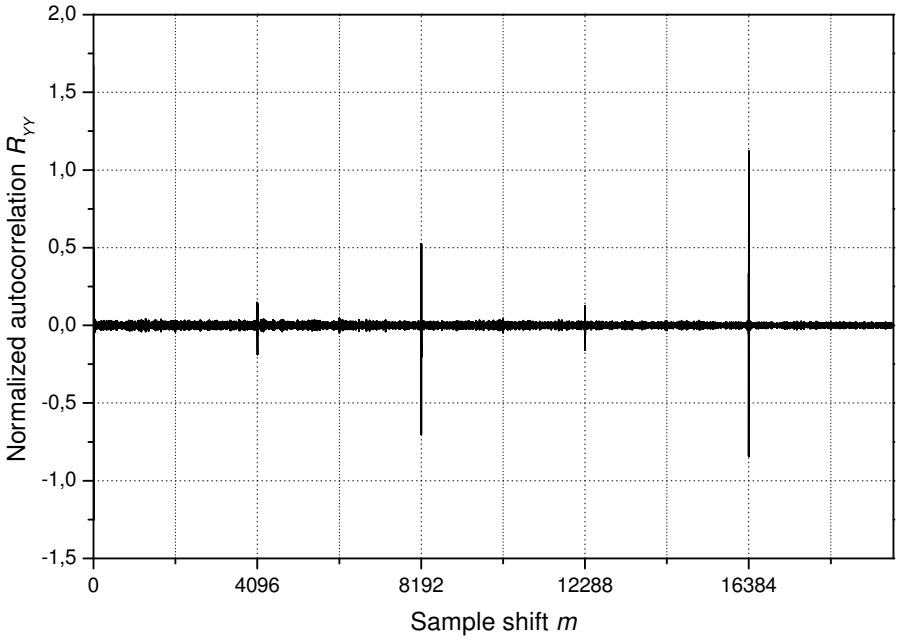


Figure 4.39: Autocorrelation estimate for the MASH 1-1-1 with DC dither in all stages; $A[n] = 0101000000_2$, $C_{1,0}[n] = C_{1,1}[n] = C_{2,0}[n] = C_{2,1}[n] = 1$

Such dithering topology generates relatively powerful 8-level dither. However, 3-rd order high-pass filtering performed by the modulator prevents noise degradation at low frequency offsets.

The concept of direct feedback dithering introduces a DC component into the quantized output signal, which seems to appear as a drawback. Indeed, feedback signal influences the modulators input as well as the average value of the output signal Y[n]. In the case of constant control signal applied to the modulator, this just slightly changes the DC component of the quantized signal. If sigma-delta modulator shown in Fig. 4.40 controls a 8 modulus prescaler with the division ratios of N, N + 1, $\cdots$, N + 7, the fractional division ratio defines as:

$$N_{frac} = N + 3 + A[n] + \frac{3 + A[n]}{2^{k+3}}, \tag{4.63}$$

where $A[n] = (A_0[n] + A_1[n] \cdot 2 + \ldots + A_{k-1}[n] \cdot 2^{k-1})/2^k = const.$

4.8.1 Linear model

The presented dithering topology comprises a feedback loop which can alter the quantization noise distribution. Moreover, feedback can become a source of in-

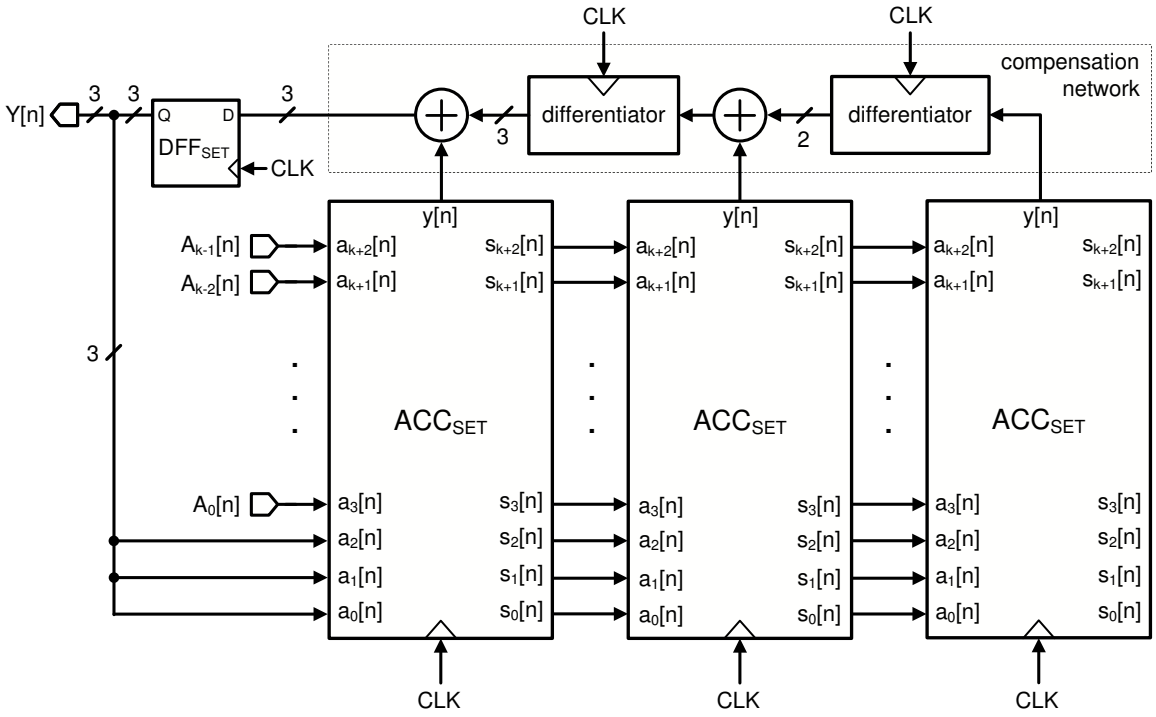


Figure 4.40: Implementation of a MASH 1-1-1 modulator with direct feedback dithering

stability of MASH modulator and degrade its tonal performance if the feedback gain exceeds some specific value.

Fig. 4.41 illustrates the linear model of a MASH 1-1-1 modulator with direct feedback dithering. The output signal is scaled by the factor of m and is fed back to the input.

The output of a MASH modulator defines as:

$$Y(z) = A_x(z) + (1 - z^{-1})^3 e_3(z) \tag{4.64}$$

The $A_x(z)$ consists of the input and feedback signals:

$$A_x(z) = A(z) + mY(z)z^{-1} \tag{4.65}$$

Substitution of (4.65) into (4.64) and rearranging yields:

$$Y(z) = \frac{A(z)}{1 - mz^{-1}} + \frac{(1 - z^{-1})^3}{1 - mz^{-1}} e_3(z) \tag{4.66}$$

Signal transfer function $H_{STF}(z) = 1/(1 - mz^{-1})$ has a low-pass characteristic, thus does not change the DC input. Noise transfer function $H_{NTF}(z) = \frac{(1-z^{-1})^3}{1-mz^{-1}}$

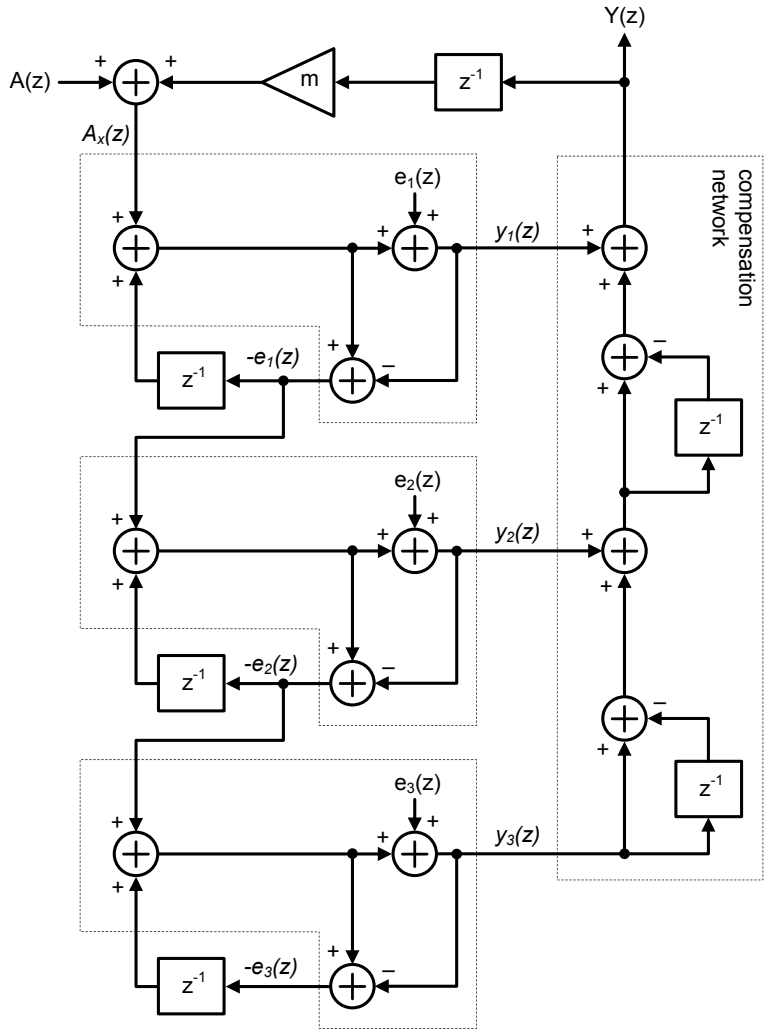


Figure 4.41: Linear model of a MASH 1-1-1 modulator with direct feedback dithering

expectedly approaches the noise transfer function of a MASH 1-1-1 for infinitesimal feedback gain m. When m grows up, noise transfer function transforms into the second order transfer function. Fig. 4.42 shows the magnitude of noise transfer function for different feedback gain values. With the increase of m the quantization noise at low frequencies goes up, while the noise at high frequencies falls down.

Such quantization noise change might seem beneficial, since 3-rd order MASH mostly degrades the phase noise of the wide-band PLL exactly at frequency offsets in the vicinity of half of the reference frequency. However, linear analysis does not show nonlinear performance of the sigma-delta modulator. Discrete-time simulation is required to evaluate the stability and tonal performance of the system.

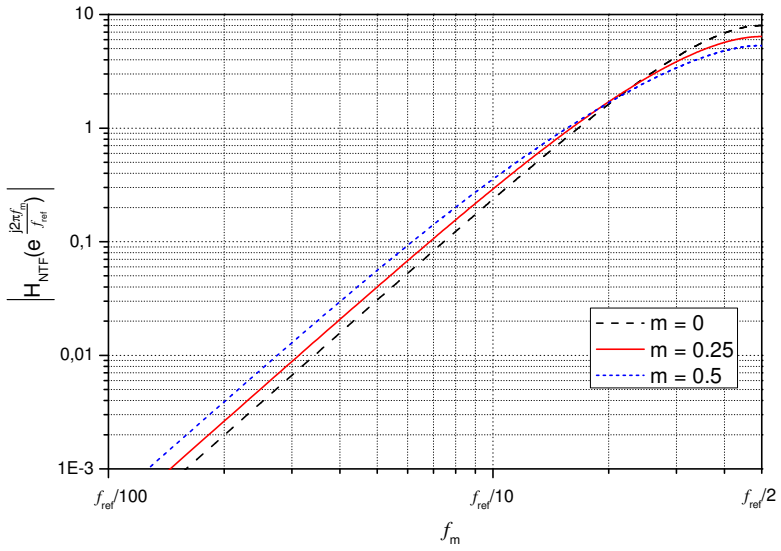


Figure 4.42: Magnitude of $H_{NTF}(z)$ of MASH 1-1-1 modulator with direct feedback dithering for different feedback gain

4.8.2 Simulation Results

To verify practically the dithering capabilities and stability issues of the presented topology a discrete time model of the dual edge triggered MASH 1-1-1 modulator employing direct feedback dither was simulated Matlab environment.

Firstly, the boundary value of the feedback gain m for which the modulator demonstrates stable, tone-free performance was estimated. This was done by exhaustive simulation of the modulator with different input and feedback gain values. Autocorrelation estimate was used to verify the modulator's performance.

According to the simulation results, the maximum value of a feedback gain for which the modulator is stable and generates reasonably smoothed quantization noise spectrum is $m = 0.0079$. The closest to 0.0079 fraction expressed in term of the power of 2 is $1/2^7 = 0.0078125$. This implies than the usage of direct feedback dithering implemented exactly at it is shown in Fig. 4.40 is possible if the resolution of accumulators is 7 bits or higher (k $\geq$ 4). Practically, the resolution of sigma-delta modulators used in frequency synthesizers exceeds 7 bits which makes this limitation insignificant. It is worth mentioning that modulator's output sequence spreads over the 3 bits and for the case of 7-bit accumulators only 4 most significant bits could be used for the input control signal.

For experimental verification the 14-bit accumulators were chosen. The resolution of the input word is 11 bits. Referring to Fig. 4.40, $k = 11$.

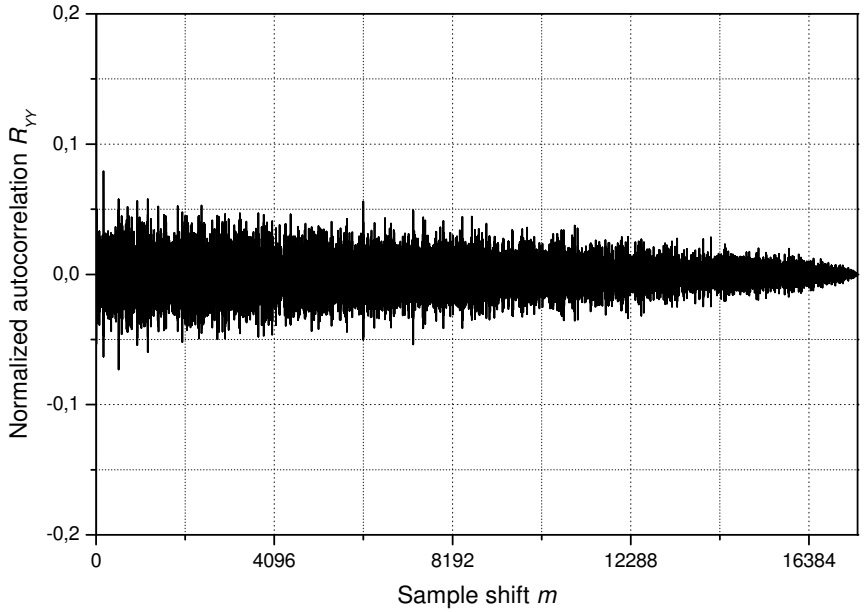


Figure 4.43: Discrete time autocorrelation estimate of the modulator output for the MASH 1-1-1 modulator with direct feedback dithering

For simulation, the static input signal A[n] = 0.25 is applied to the input of MASH modulator. The autocorrelation of the output calculated from 40000 samples is shown in Fig. 4.43. The estimate is relatively smoothed and only some insignificant periodicity is visible. Repeated simulations for the other values of input signal demonstrated similar autocorrelation estimate.

The quantization noise change caused by the influence of feedback dithering signal is very insignificant and it is assumed that the modulator has the same quantization noise distribution as a conventional MASH 1-1-1 structure.

Thus, simulation showed the efficiency of direct feedback dithering in MASH 1-1-1 modulator. In spite of the fact that modulator generates sequence with little periodicity, the absence of additional hardware for implementation of such dithering topology makes direct feedback dithering an attractive choice for using in compact, low switching noise, integrated modulators for frequency synthesis applications.

4.9 MASH 1-1-1 Modulator with Oscillator-Based Dithering

Oscillator-based dither generation is a trade-off between the direct feedback dithering, which requires no additional hardware, and pseudo-random noise generator commonly used for dither generation purposes. The latter efficiently suppresses the tones in sigma-delta modulator but requires at least 10 D-flip-flops (this was demonstrated by means of simulations in Section 4.5.4). Direct feedback dithering method requires no hardware, but it shifts the DC value of the output sequence and leaves some low-amplitude spikes in the discrete time autocorrelation estimate.

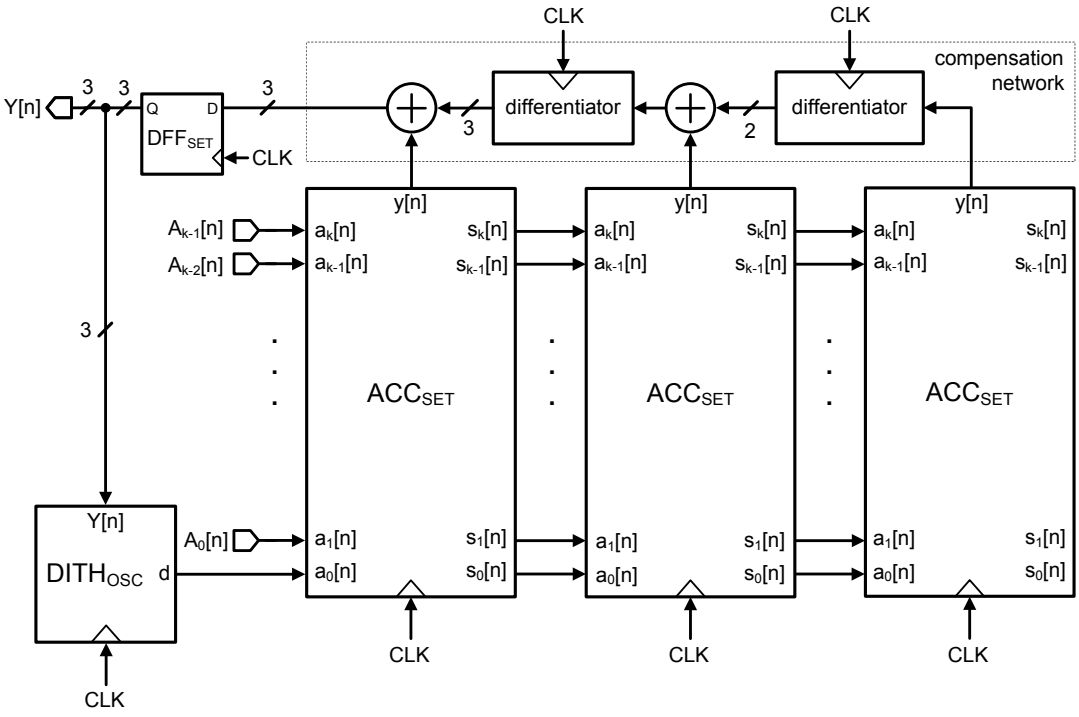


Figure 4.44: MASH 1-1-1 modulator with oscillator-based dithering

The basic idea of the second topology is to use oscillator with a high phase noise for dither generation. The block diagram of a MASH 1-1-1 modulator with oscillator-based dithering is shown in Fig. 4.44. The schematic diagram of the oscillator-based dither generator (block DITH_{OSC}) is shown in Fig. 4.45. It consists of the voltage controlled ring oscillator, output signal of which is triggered with a reference frequency and applied to the modulator input. Thus, the 1-bit random signal is generated and applied to the least significant bit of the first stage a_0[n]. In order to further randomize the dither and exclude any spurious emission due to the correlation between ring oscillator frequency and a reference

frequency, the oscillator is tuned at each reference cycle by the 3-bit modulator's output signal Y[n]. Transistors M_1, M_2, and M_3 perform a role of varactors. Oscillation frequency is chosen to be several times higher than the reference frequency. Specifically, the tuning range of the implemented oscillator lies between 230 MHz and 330 MHz.

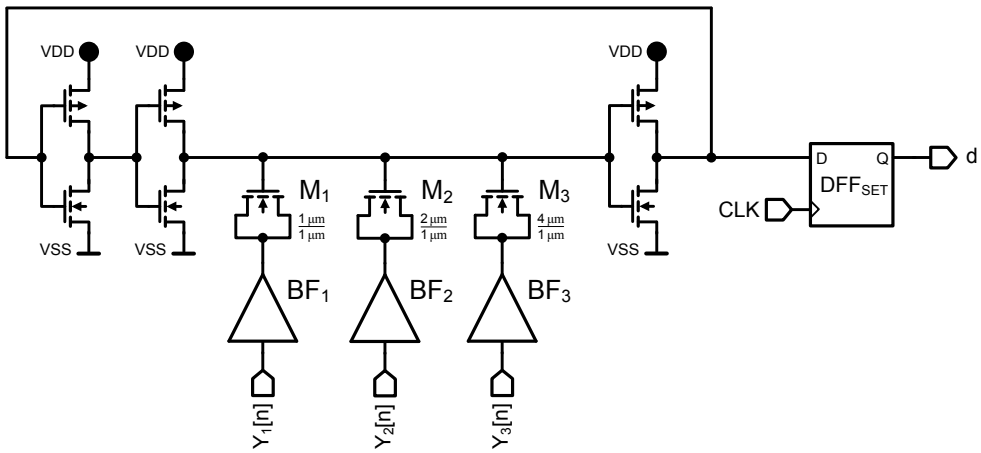


Figure 4.45: Voltage controlled ring oscillator used as a dither generator (block DITH_{OSC} in Fig. 4.44)

The spectrum of the generated dither should be analyzed to ensure that, on one hand, it is able to smooth quantization noise spectrum and, on the other, does not degrade overall PLL phase noise or tonal performance. Fig. 4.46 shows the spectral content of oscillator-based dither. The oscillator carrier is frequency-modulated by the output signal of sigma-delta modulator. The output signal of the modulator, which is a high-pass, discrete-time signal quantized with a reference frequency, after modulation appears as the sidebands at both sides of the ring oscillator carrier. In the implemented ring oscillator wide-band modulation takes place, namely $m = \Delta f / f_{ring} > 0.3$, where f_{ring} is the frequency of the free running oscillator, Δf is the maximum frequency deviation.

As it is shown in Fig. 4.46, the VCO frequency is chosen to be several times higher than the reference frequency. After quantization of the modulated VCO carrier with a sampling frequency f_{ref}, VCO carrier together with a sidebands fall into the frequency band $[0; f_{ref}/2]$. Due to the aliasing, the spectrum in $[0; f_{ref}/2]$ band contain quantization noise with close to the white distribution and oscillator's carrier. In Fig. 4.46 the rough view of the amplitude spectrum of quantized signal up to the frequency $f_{ref}/2$ is demonstrated. The performed simulations showed that after aliasing quantization noise indeed has white distribution. In [Chou 91] it was proved that digital MASH 1-1-1 modulator generates white quantization error if identically distributed (white) dither is applied to the modulator. Based on the assumption that oscillator-based dither generator produces noise with

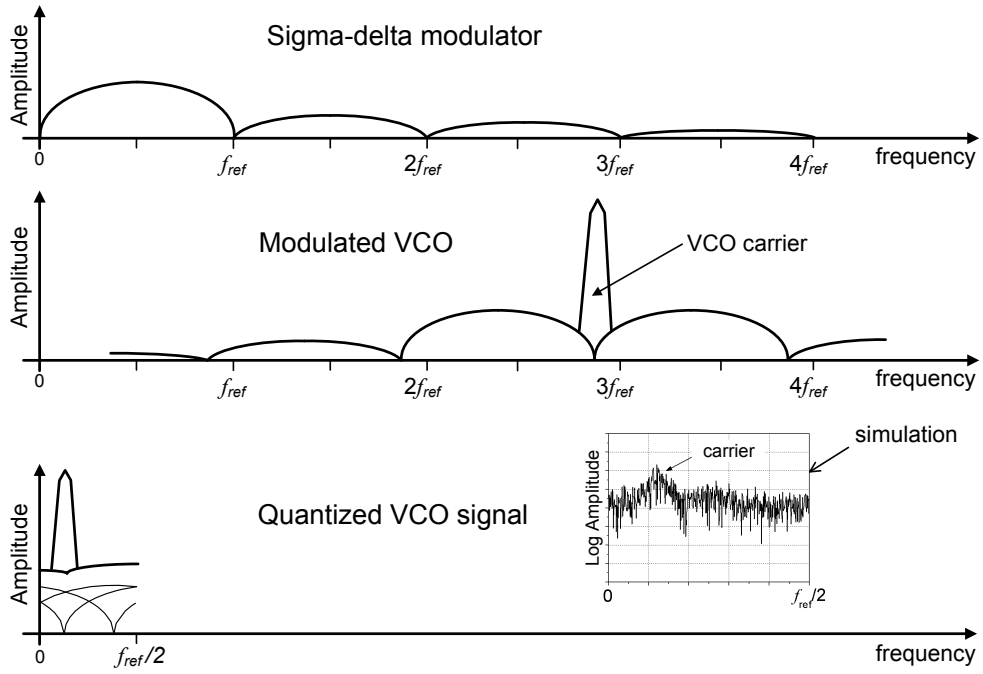


Figure 4.46: Spectral content of oscillator-based dither

close to the white distribution, such dithering topology can efficiently smooth quantization noise spectrum of the MASH 1-1-1 modulator.

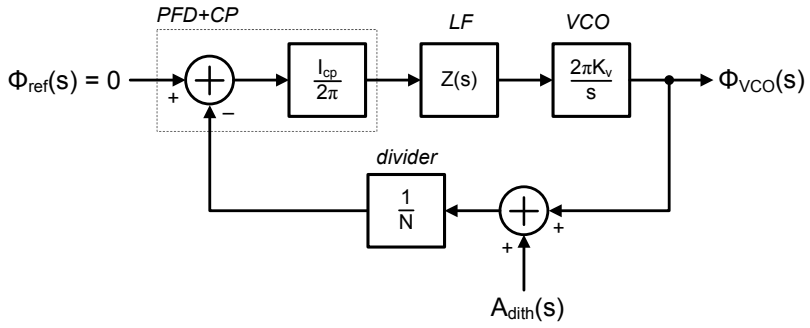


Figure 4.47: PLL linear model

Besides the quantization noise, dither contains also a VCO carrier which can be transformed into the spur in overall PLL output spectrum. Thus, the analysis is required to estimate the power of the spur produced by the oscillator-based dither generator. For simplifying the analysis, 1 LSB dither and the worst case carrier amplitude of 1 LSB peak-to-peak are assumed. In reality the carrier amplitude will be lower, since part of the energy is concentrated in the sidebands; for the case of frequency modulation, the total energy stored in the carrier and in the sidebands is constant [Young 94].

The PLL linear model where the signal from dither generator and consequently from sigma-delta modulator is induced into the loop is shown in Fig. 4.47. $A_{dith}(s)$ represents the signal of oscillator-based dither generator, which is added into the loop exactly after the VCO. A transfer function from the input to the VCO output defines as:

$$H(s) = \frac{\Phi_{VCO}(s)}{A_{dith}(s)} = -\frac{I_{cp}Z(S)K_v/N}{s + I_{cp}Z(S)K_v/N} \tag{4.67}$$

Thus, the phase deviation at the output of the VCO is

$$\Phi_{VCO}(s) = H(s)A_{dith}(s) \tag{4.68}$$

Transforming phase deviation into the spurious tones at the output of PLL expressed in dBc [Vaucher 02], we obtain:

$$P_{dith}(\Delta f) = 20\log\left(\frac{|H(j2\pi\Delta f)A_{dith}(j2\pi\Delta f)|}{2}\right) \tag{4.69}$$

The magnitude of the $H(s)$ within the PLL bandwidth is 1. Outside the PLL bandwidth $|H(s)|$ rolls down. The amplitude of A_{dith} at the frequency of quantized ring oscillator carrier is $1/2 \cdot 2^{k+1}$ (it spreads over 1 LSB), where $k+1$ is a modulator's resolution, as shown in Fig. 4.44. Substituting this into (4.69) we obtain the spur power depending on the modulator's resolution (the magnitude of H(s) at the frequency of quantized ring oscillator is assumed):

$$P_{dith}(k) = 20\log\left(\frac{|H|\,2^{k+1}}{4}\right) \tag{4.70}$$

The worst case spur power will occur if harmonic falls into the PLL bandwidth, where $|H(s)| = 1$. Fig. 4.48 demonstrates the spur power occurred within the PLL bandwidth over the resolution of sigma-delta modulator. For the resolutions more than 10, the spurious tone power is well below –70 dBc.

4.9.1 Simulation Results

The simulation of a MASH modulator comprising oscillator-based dither generator was performed in Agilent ADS 2006 environment. ADS features the possibility to perform mixed-signal simulations which appear to be much faster than the modeling of pure analog circuits. MASH modulator was built using Verilog-A-based model, while oscillator-based dither generator is represented by the circuit-level model. The latter cannot be simulated as a discrete-time system, since it employs fully analog voltage-controlled oscillator. MASH 1-1-1 modulator core is implemented in a dual edge triggered style.

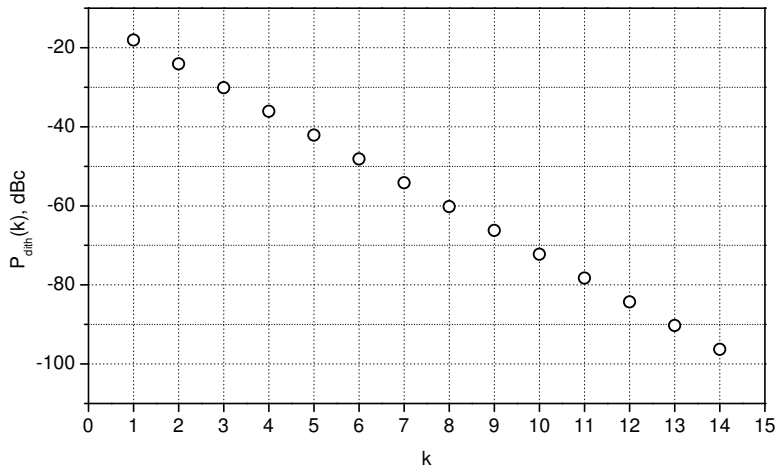


Figure 4.48: Spur power versus modulator's resolution

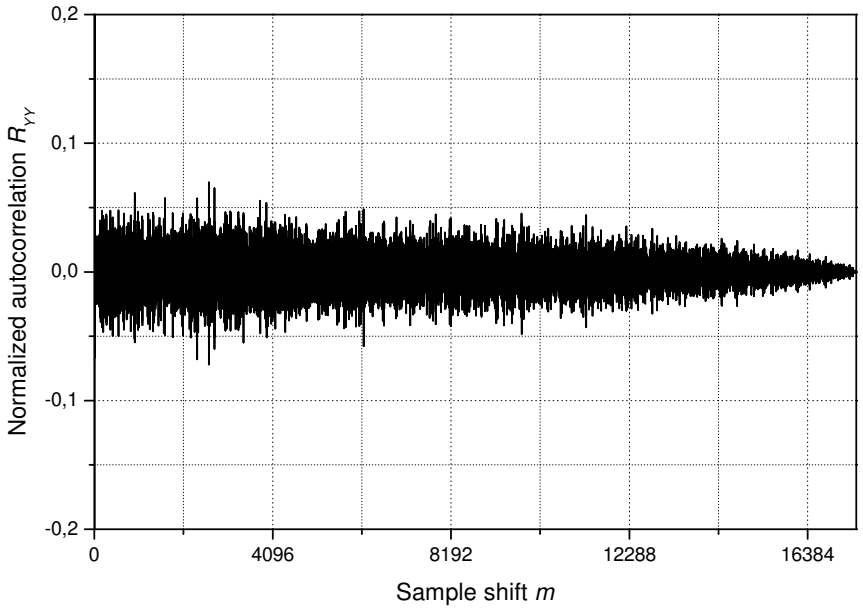


Figure 4.49: Discrete time autocorrelation estimate of the modulator output for the MASH 1-1-1 modulator with oscillator-based dither generator

The autocorrelation estimate calculated from 40000 samples is demonstrated in

Fig. 4.49. It does not contain any powerful spikes which proves the efficiency of oscillator-based dither generator in smoothing the quantization noise of MASH 1-1-1 modulator.

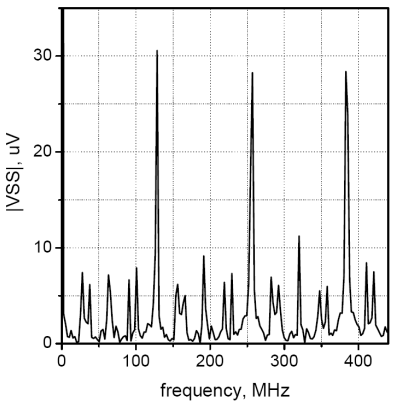
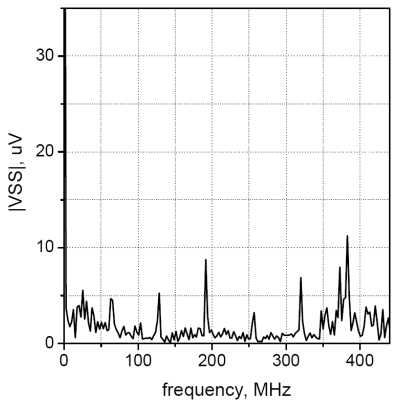
	10-bit pseudo-random generator	Oscillator-based dither generator
Amplitude spectrum of supply voltage		
Current consumption	269 µA	54 µA
Occupied area	378 µm^2	180 µm^2

Figure 4.50: Comparison of oscillator-based dither generator with conventional 10-bit pseudo-random generator

When compared to the autocorrelation estimate of MASH modulator with direct feedback dithering, oscillator-based dither generator demonstrates better spurious performance. Conventional pseudo-random dither generator can provide the same spurious suppression only if its resolution is 10 bits or higher.

Another set of simulations were carried out to estimate hardware efficiency of the oscillator-based dither generator. The results were compared with the 10-bit pseudo random generator, since their efficiency in modulator's quantization noise whitening is similar. The results of comparison are summarized in Fig. 4.50.

A supply network scheme shown in Fig. 4.32 was used for simulating the perturbations on the ground nodes. Generators were triggered with a reference frequency $f_{ref} = 64$ MHz. The harmonics in amplitude spectrum of oscillator-based dither generator are more than 3 times lower than for pseudo-random generator. This is explained by the fact, that oscillator-based dither generator contains only one D-flip-flop instead of 10 flop-flops in pseudo-random generator. Moreover, the internal signal of the oscillator is not correlated with the reference frequency which makes the spikes in amplitude spectrum of VSS voltage to be non-harmonically related with the reference spikes.

Oscillator-based dither generator demonstrated 5 times lower current consumption and 2 times reduced area than its counterpart.

Chapter 5

11 GHz PLL Core Implementation

5.1 Technological Framework

11 GHz PLL core together with the integrated sigma-delta modulator are realized in Infineon 0.13 μm C11RF technology.

C11RF is a twin well CMOS technology on non-epi p^- substrate. Fig. 3.6(a) demonstrates an approximate substrate cross section. The resistivity of the substrate is 20 Ω-cm.

In order to reduce the conductivity of substrate, p-well implant under the passive inductors/transformers structures is blocked by placing the moat mask. Also, as it is shown in Fig. 3.9, with the help of moat mask the conductive path formed by p-well between different regions of the substrate can be broken. This serves as a feature for reducing the amount of digital noise coupling.

The technology offers thin gate oxide MOS transistors with a minimum drawn gate length of 0.12 μm and three different threshold voltages: low-V_t, regular-V_t, and high-V_t. Threshold voltage of a regular-V_t NMOS transistor is approximately 0.4 V. Low-V_t and high-V_t transistors have around 0.1 V lower/higher threshold voltage than that of regular-V_t NMOS. For input/output circuits thick gate oxide MOS transistors can be used. Their gate oxide breakdown voltage is twice higher than in thin gate oxide MOSFETs. Additionally, C11RF technology offers *pnp* bipolar transistor used mainly for bandgap reference design.

Most of the MOS devices used in the PLL are regular-V_t transistors. Some analog blocks comprise low-V_t MOSFETs. High-V_t are not used in the design. Input ESD structures are implemented in thick gate oxide MOSFETs.

Metallization stack consists of 6 layers: 4 lower levels are thin copper metals and 2 upper levels are thick copper-aluminium metals. The uppermost metal-

lization layer has the highest thickness and is used for high-Q passive inductors/transformers design.

MIM (Metal-Insulator-Metal) capacitors offered by C11RF technology are of high importance in integrated PLL design. They have tighter tolerance and higher capacitance per unit area than metal-to-metal parallel plate capacitors. Since the loop filter can comprise relatively large capacitors, the use of MIM structures can save a significant fraction of die area, lowering the cost of the device (even in spite of the fact, that fabrication of MIM capacitors require additional lithography masks). Moreover, MIM capacitors are built between the two uppermost metallization layers, which makes the parasitic capacitance between the bottom plate and the substrate insignificant. This serves as a useful feature when the minimum substrate noise coupling is desired.

Among the variety of resistors offered by the technology, polysilicon resistors with blocked salicidation are the most widely used in the PLL design. While having sheet resistance high enough to lay out the compact structures, the tolerance of polysilicon resistors is also reasonably low. The tolerance is inversely proportional to the area of resistor: the larger the area the more accurate will be the value of a fabricated resistor.

The nominal supply voltage is 1.5 V.

For more details concerning the technology the user is referred to [Debski 07], [Vasylyev 06], were the hardware was fabricated under the same 0.13 μm C11RF process.

5.2 PLL Linear Model

A PLL linear model is used for calculating the AC response of the loop and output phase noise distribution [Craninckx 98]. Each block of the PLL is represented by the lumped element circuit model in phase domain and includes the sources (if any) contributing the noise to the phase-locked loop by this block.

The VCO model shown in Fig. 5.1 transforms the input tuning voltage into the output phase deviation. The capacitance at the tuning terminal C_t = 500 fF represents varactor capacitance together with layout parasitics and is included into the model since its value is comparable with the output capacitance of the loop filter. Resistance R_t = 100 MΩ models leakage current in varactor.

The current source controlled by the voltage together with the capacitance C_v perform the integration action of the VCO when converting tuning voltage to the phase:

$$\Phi_{VCO}(s) = \frac{1}{C_v s} V_{tune}(s) \tag{5.1}$$

The capacitance has the value of

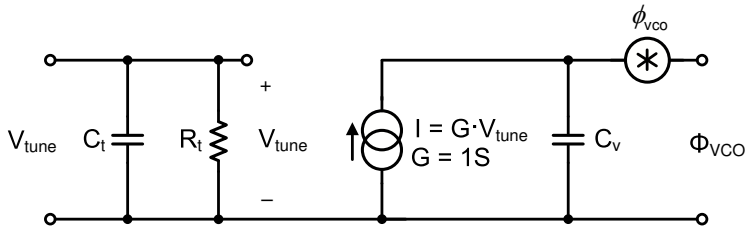


Figure 5.1: VCO linear model in phase domain

$$C_v = \frac{1}{2\pi K_v} \tag{5.2}$$

where K_v is a VCO gain measured in GHz/V and its value can be taken from Fig. 5.9 depending on the VCO operating point (namely, tuning voltage).

The definition of the single sideband phase noise root spectral density ϕ_{vco} is given by (5.5). Since resistance R_t models just the effect of leakage current and does not exist in the circuit as the real resistor, it generates no thermal noise.

Phase-frequency detector together with a charge pump perform phase difference-to-current conversion. Referring to linear model of PFD/CP in Fig. 5.2, the two input voltage sources controlled by the voltage perform the subtraction of divided signal from the reference and then current source controlled by the voltage transforms this difference to the charge pump current. Since all the phases in linear model are measured in radians and I_{cp} equals the charge pump average current for the maximum input phase difference, i.e. 2π, I_{cp} is divided by 2π in the definition of charge pump current source. This gives a PFD/CP gain measured in the units of [A/rad]. The average output charge pump current is denoted as $\overline{I_{cp}}$.

The phase noise of the phase-frequency detector is modeled by the ϕ_{pd} source and charge pump noise is modeled by current noise source i_{cp}. In Section 5.3.2 the definition of ϕ_{pd} and i_{cp} is given. Resistances at the input terminals of the block are noiseless.

The linear model of a frequency divider simply divides the input frequency as well as the phase by the constant division modulus N [Craninckx 98]. The model is illustrated in Fig. 5.3. For the simplicity of the overall model, the phase noise of the divider is not taken into account. This does not significantly alter the total noise of the system, since divider's noise contribution is much weaker than the noise contribution of the VCO, charge pump, and sigma-delta modulator. The input resistor generates no noise.

Since a loop filter is already a linear circuit, its time domain model transforms into the phase domain model without a change. A third order transimpedance filter is used in the PLL. The details of its circuit implementation are given in Section 5.3.4. The noise sources $v_{n.R2}$ and $v_{n.R3}$ are described by (5.28) and (5.29).

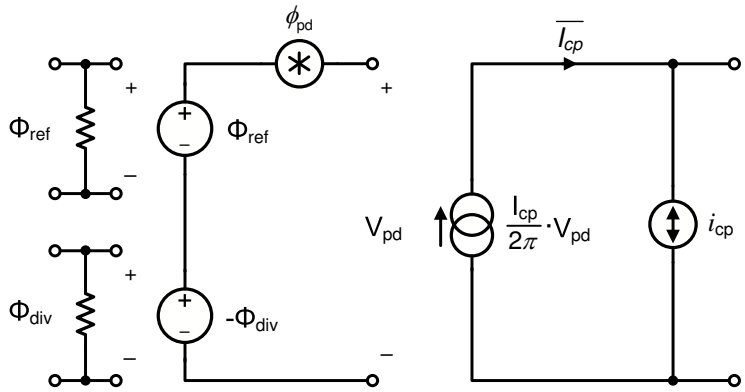


Figure 5.2: Phase-frequency detector and charge pump linear model

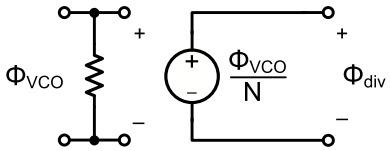


Figure 5.3: Frequency divider linear model

Finally, Fig. 5.4 illustrates the phase domain model of a full sigma-delta PLL.

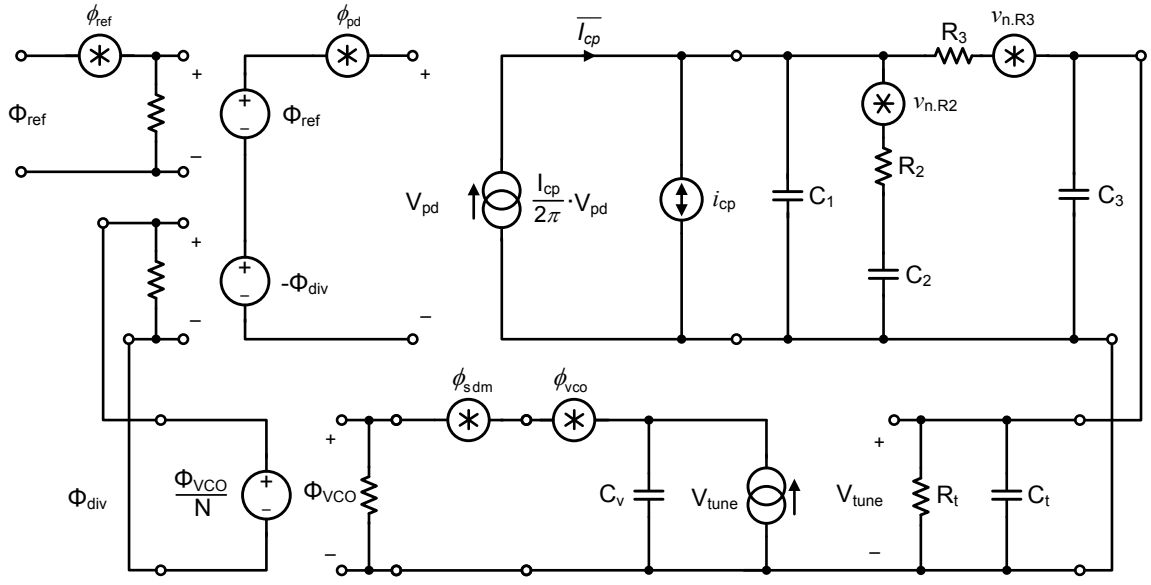


Figure 5.4: Full sigma-delta PLL linear model

5.2.1 Simulation Results

The PLL bandwidth is chosen to be 500 kHz when operating in fractional-N mode and 2 MHz when operating in integer-N mode. For obtaining a bandwidth of 500 kHz the charge pump current is set to 11 μA and the resistor R_2 of the loop filter to 45 kΩ. For changing the bandwidth to 2 MHz the charge pump current is set to 220 μA and the resistor R_2 to 15 kΩ.

Fig. 5.5 shows the simulated open- and closed loop transfer functions of the PLL for 500 kHz bandwidth. The VCO is supposed to operate at 11 GHz, resulting is a small-signal gain of 1.2 GHz/V. The phase margin of 56° provides optimum tradeoff for achieving fast locking time on one hand, and stability of the loop on the other.

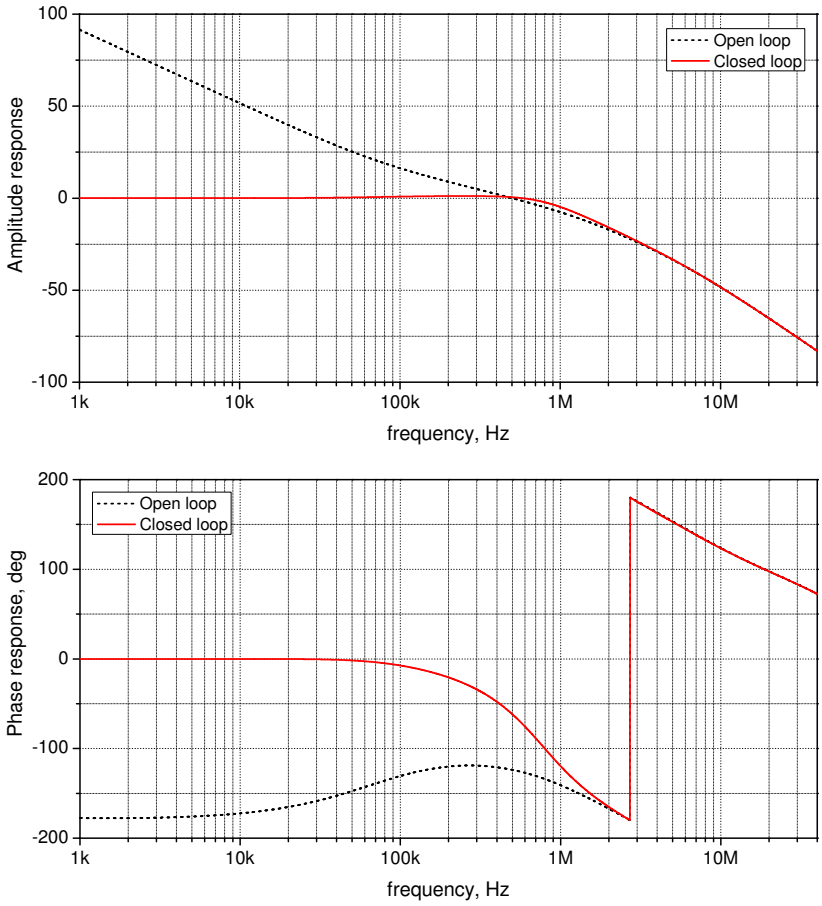


Figure 5.5: PLL transfer function for 500 kHz bandwidth

Fig. 5.6 demonstrates simulated phase noise of the PLL in integer-N mode using the linear model. Because the bandwidth is very high, PLL efficiently suppresses

the in-band noise of the charge pump, thus resulting in a total phase noise below –90 dBc/Hz. The relatively good in-band noise suppression is achieved at the expense of reduced phase margin, which results in a phase noise overshoot in the vicinity of cut-off frequency.

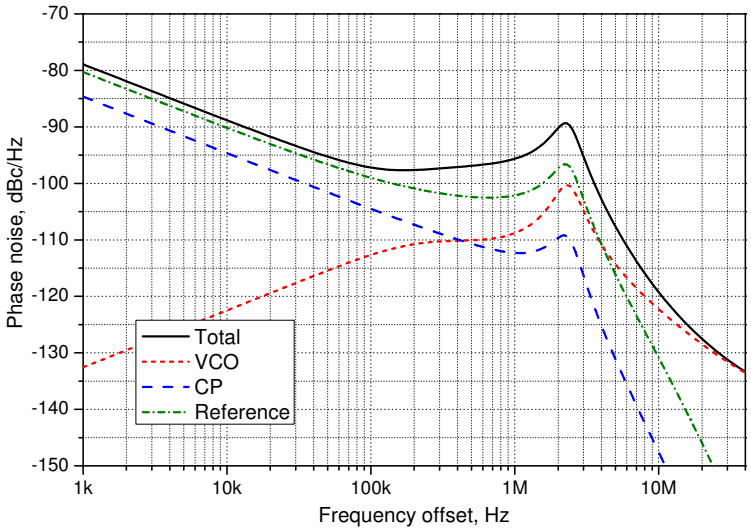


Figure 5.6: Simulated phase noise of the PLL operating in integer-N mode

The simulated phase noise of the PLL operating with a sigma-delta modulator in shown in Fig. 5.7. In order to suppress quantization noise of a sigma-delta modulator at high frequency offsets the PLL bandwidth is set to 500 kHz. With such bandwidth the noise within the offset frequency range from 6 MHz to 40 MHz is almost not degraded. The in-band noise is around 10 dB higher than in the case of fractional-N PLL. This happens firstly, due to the 4 times lower bandwidth, and secondly, due to increased charge pump noise caused by the higher duty cycle of the phase-frequency detector pulses. The sigma-delta modulator's in-band noise degradation due to the nonlinear effects is not taken into account in the model.

5.3 Circuit Implementation

5.3.1 Voltage-Controlled Oscillator

The circuit diagram of the integrated cross-coupled multivibrator VCO is demonstrated in Fig. 5.8. It consists of NMOS and PMOS differential latches, which provide a negative resistance for sustaining oscillation. Differential structure provides high immunity against the substrate crosstalk.

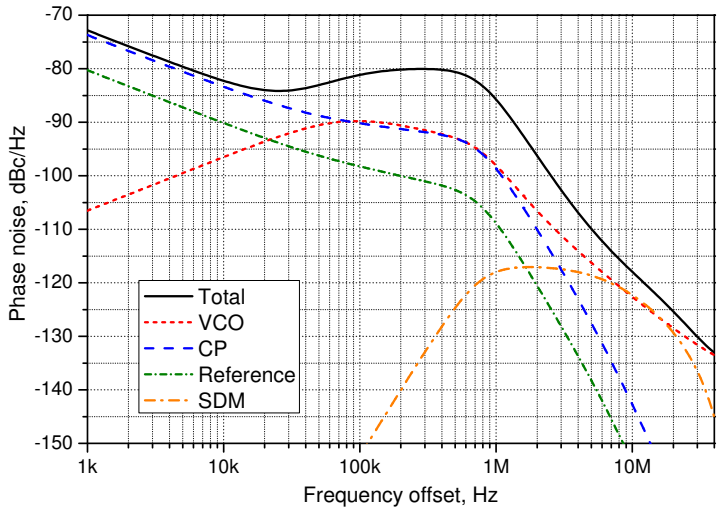


Figure 5.7: Simulated phase noise of the PLL operating in fractional-N mode

Generating 11 GHz signal, the VCO is tuned by means of a single wideband differential NMOS varactor, which can change the output frequency over 900 MHz. This results in a 8.4% tuning range. Since only one varactor is used to tune the VCO over the whole frequency range, it provides a very high gain, reaching the peak value of 1.4 GHz/V. This makes the VCO very sensitive to any perturbations coming from the loop filter or coupling into the integrated coil or active part of the oscillator through the substrate, thus, sigma-delta modulator's digital noise can easily be sensed. Fig. 5.9 shows the measured VCO tuning characteristic and gain.

As an inductor for VCO the integrated octagonal spiral coil with three windings is used. Fig. 5.10(a) shows the side view on the inductor. Each turn is winded with semi-pattern lines of three upper metallization layers connected in parallel for reducing the series resistance of the coil. The outer radius is 110 μm. Center tap of the coil is connected to AC ground and serves for controlling DC biasing of the cross-coupled pairs.

The S-parameter model of the inductor is obtained using ADS Momentum electromagnetic simulator. Estimated inductance is 0.9 nH, DC series resistance is 4.28 Ω.

Using S-parameter model the Q-factor of the inductor was estimated. Instead of the widespread definition of quality factor as a ratio of imaginary to real part of the input admittance, bandwidth method for quality factor estimation is used [Maget 02]. Since inductor together with a varactor are operating at resonance in the VCO, this method provides practically reasonable results. The ideal ca-

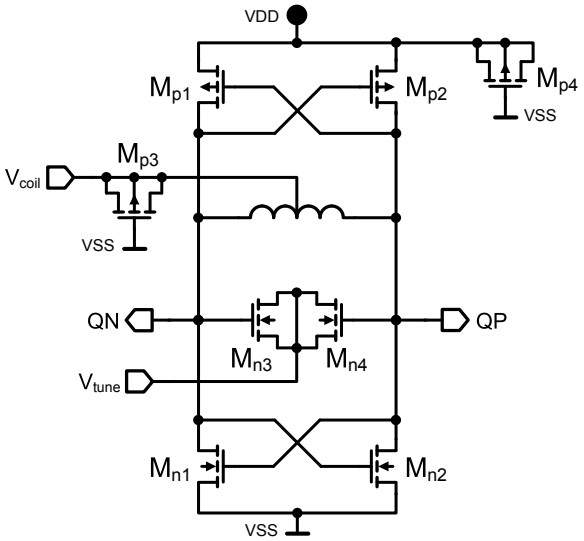


Figure 5.8: VCO circuit diagram

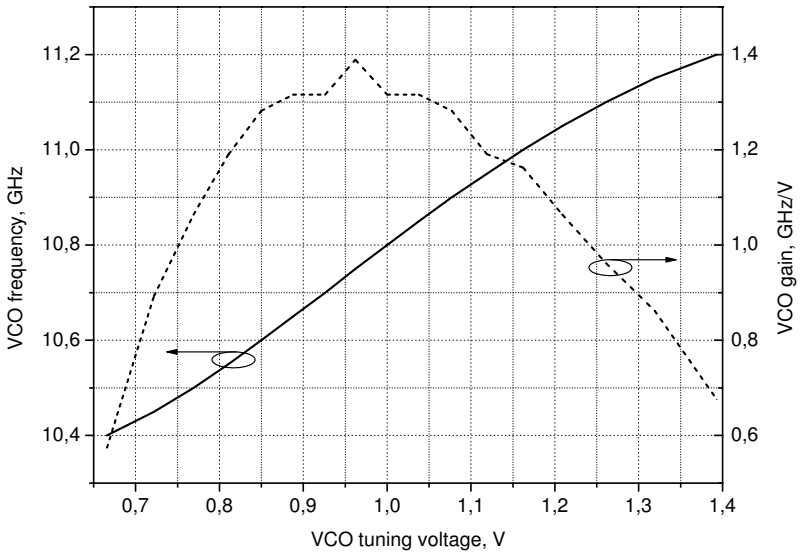


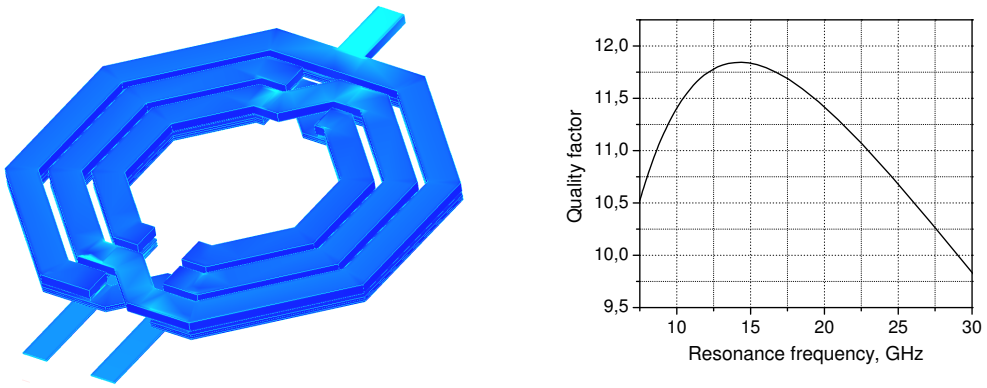
Figure 5.9: Measured VCO tuning curve and gain

pacitance is added in parallel to the inductor model and impedance of the tank is calculated. The magnitude of impedance has a bandpass characteristic and Q-factor for the resonance frequency f_0 defines as

$$Q = \frac{f_0}{\Delta f_{3dB}}, \tag{5.3}$$

where Δf_{3dB} is a 3 dB bandwidth of the amplitude response of the tank.

Estimated quality factor versus resonance frequency is depicted in Fig. 5.10(b). It reaches the maximum of 11.85 at resonance frequency of 14 GHz. At the VCO oscillation frequency which equals 11 GHz the Q-factor is slightly lower, namely 11.6.



(a) (b)

Figure 5.10: (a) – VCO inductor view, (b) – simulated quality factor of the inductor

In order to provide 8.4% tuning range with only one varactor, the size of transistors M_{n3} and M_{n4} is chosen to be W/L = 64μm/0.24μm. Such relatively large transistors provide an input capacitance of 500 fF at V_{tune} terminal. This value is comparable with the output capacitance of the loop filter and included into the high level model of the VCO used for behavioral simulation of the PLL.

Because of the distributed structure of a channel of MOS transistor and finite gate sheet resistance, varactor always has some resistance in series with the capacitance. In order to maximize the quality factor of a varactor, series gate resistance must be minimized. Transistors M_{n3} and M_{n4} are broken into 8 fingers for reducing series gate resistance R_{gate}, which is proportional to [Maget 02]

$$R_{gate} \propto \frac{F_\square R_\square}{N_F} \tag{5.4}$$

where $F_\square$ is the number of squares per finger, $R_\square$ – gate square resistance, N_F – number of parallel fingers.

Moreover, for further reduction of R_{gate}, each gate finger in the layout is connected to the metal with both sides. When the gate is contacted at two sides its resistance

is four times lower than in one-side contacted gate [Debski 07]. Simulation showed that two-sided contact to the gate reduces the VCO phase noise by around 1 dB at frequency offsets above 1 MHz. The same layout style is applied to the cross-coupled active pairs.

The VCO is loaded with the buffer (Fig. 5.11) and high-frequency divider implemented in current mode logic, see Fig. 5.26. The buffer performs a role of an output pad driver. The VCO was simulated together with the buffer and divider, since they significantly influence its oscillation frequency and phase noise. The phase noise simulation was performed in ADS environment using harmonic balance analysis. The result is shown in Fig. 5.12. The phase noise curve simulated with $V_{tune} = 0$ V represents the lowest noise level generated by the free-running VCO, while the curve for $V_{tune} = 0.7$ V shows the highest phase noise level. For any other tuning voltages phase noise curves will lie in between these two.

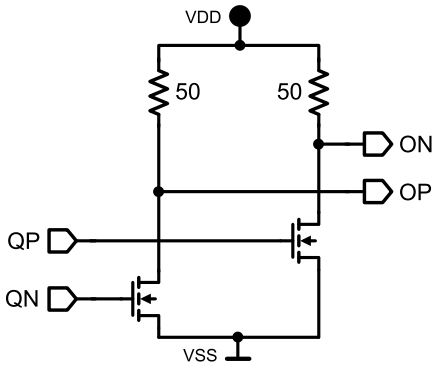


Figure 5.11: VCO buffer circuit diagram

In the same diagram measured phase noise of the free-running VCO is presented. In order to measure the phase noise of the VCO integrated into PLL reference signal is disconnected from the PLL and it is driven into out-of-lock state. Charge pump is constantly sinking the current out of the loop filter, thus holding the VCO tuning voltage almost at zero. For such operating conditions phase noise diagram is shown in Fig. 5.12; carrier power is –16 dBm. The difference between simulated and measured phase noise does not exceed 3 dB over the whole offset range.

For reducing the influence of external supply noise and noise coming from the digital blocks of the chip, VDD and V_{coil} terminals are blocked with capacitively-connected PMOS transistors M_{p3} and M_{p4}. The first one biased with a voltage above 0.7 V provides a small-signal capacitance of around 87 pF, the second one connected between VDD and VSS has a capacitance of 26 pF. Gates of M_{p3} and M_{p4} are divided into several hundred fingers W/L = 4μm/1.2μm each. In parallel to capacitively-connected PMOS transistors the 4-layer polysilicon-to-metal and metal-to-metal parallel plate capacitors are added and placed above the transistors in layout. The whole blocking structure is distributed around the VCO core. Such layouting breaks the *p*-well, replacing it with capacitive path

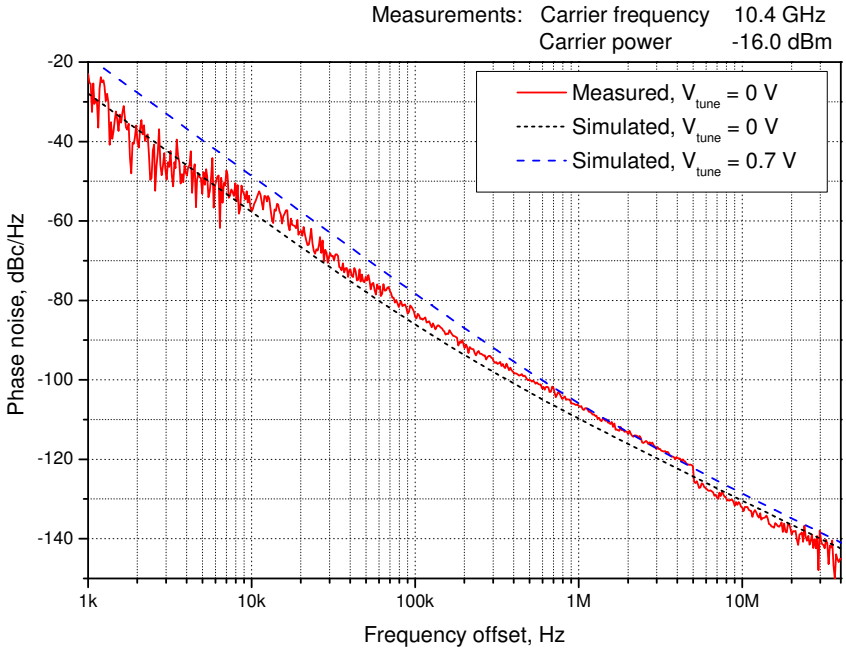


Figure 5.12: Free running VCO single sideband phase noise

formed by the reverse biased n-well-to-substrate pn-junction, thus reducing the amount of switching noise coupled into the VCO.

Phase Noise Approximation

An asymptotic phase noise approximation is done in order to represent the single sideband (SSB) phase noise of the VCO by a simple function rather than numerically. The approximation in used further in the linear model of a PLL. The diagram in Fig. 5.13 approximates the VCO phase noise shown in Fig. 5.12. The corner frequency Δf_{c3} is 200 kHz which is clearly visible from Fig. 5.12.

The function for approximating the single sideband phase noise root spectral density of the VCO looks as follows:

$$\phi_{vco}(\Delta f) \approx \sqrt{2 \cdot \left(10^{\frac{\mathcal{L}_0}{10}} + 10^{\frac{\mathcal{L}_{b2}(\Delta f)}{10}} + 10^{\frac{\mathcal{L}_{b3}(\Delta f)}{10}}\right)} \tag{5.5}$$

where

$$\mathcal{L}_{b2}(\Delta f) = \mathcal{L}_2 + 20 \log \frac{\Delta f_2}{\Delta f} \tag{5.6}$$

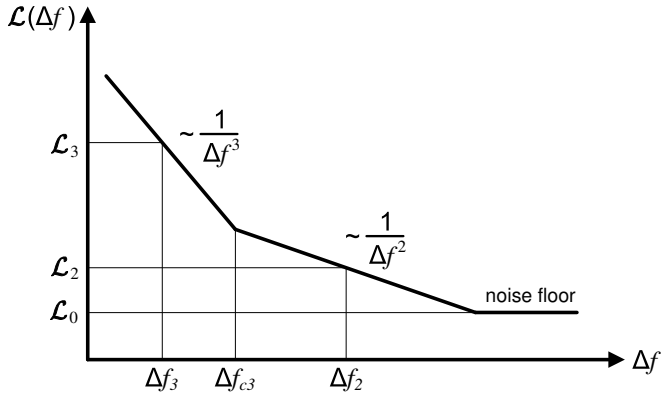


Figure 5.13: Asymptotic approximation of the VCO phase noise

Table 5.1: Values for phase noise approximation

Frequency offset		**Phase noise**	
Δf_3	100 kHz	$\mathcal{L}_3$	–77 dBc/Hz
Δf_2	10 MHz	$\mathcal{L}_2$	–128 dBc/Hz
		$\mathcal{L}_0$	–140 dBc/Hz

$$\mathcal{L}_{b3}(\Delta f) = \mathcal{L}_3 + 30 \log \frac{\Delta f_3}{\Delta f} \tag{5.7}$$

The numerical values of phase noise at corresponding frequency offsets used in (5.5), (5.6), and (5.7) are listed in Table 5.1.

5.3.2 Phase-Frequency Detector and Charge Pump

As a phase error-to-current converter dead-zone free sequential phase-frequency detector [Vaucher 02] together with a current steering charge pump [Rhee 99] are used.

Fig. 5.14 demonstrates phase-frequency detector circuit diagram. NAND gates and inverters are implemented in differential push-pull cascode logic (PPCL) [Heller 84]. All the terminals and wires in the diagram are differential: REF terminal consists of REFP and REFN, UP terminal consists of UPP and UPN and so on. The inverters drawn with a dashed line are not presented in the circuit and their function is implemented just by swapping the phases of differential signal. Inverters at the UP and DOWN outputs, however, are presented in a PFD and used mainly as the buffers. The realization of NAND gate and inverter is shown in Fig. 5.15.

Being fully differential, PPCL logic is significantly protected from the common mode substrate noise influence, resulting in a low jitter of the output pulses. The

PFD generates highly symmetrical edges which is important for improving the switching characteristics of a charge pump. Among the side benefits of PPCL implementation is the lower power consumption than offered by CMOS implementation [Dalt 02].

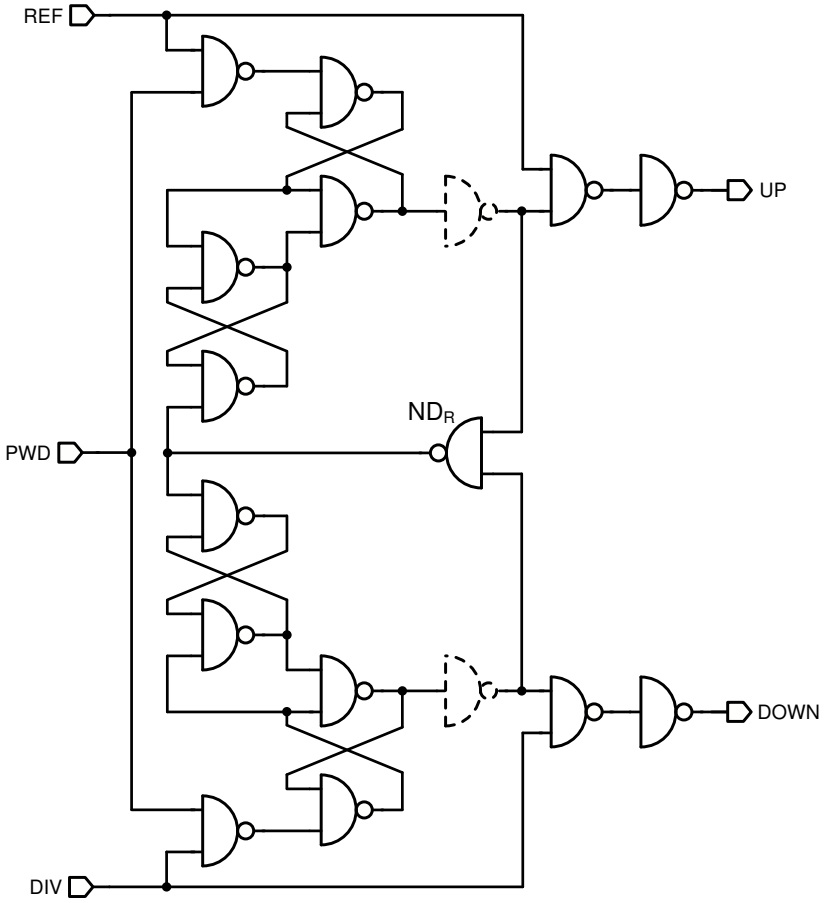


Figure 5.14: Sequential phase-frequency detector implementation

The absence of dead zones in phase-frequency detector is achieved by insertion of short pulses at UP and DOWN terminals when the phase difference of the input signals is zero. The pulse width determines by the propagation delays in reset NAND gate ND_R and flip-flops. With the help of simulation the UP and DOWN pulses width under the locked conditions (zero phase different between reference and divided signals) was estimated: 0.2 ns.

An important parameter used later for charge pump noise calculation is the duty cycle of the UP and DOWN pulses under the locked conditions. It defines as

$$\delta_{lock} = t_{lock} f_{ref}, \tag{5.8}$$

where t_{lock} is a pulse width generated by the PFD when the PLL is in lock, f_{ref}

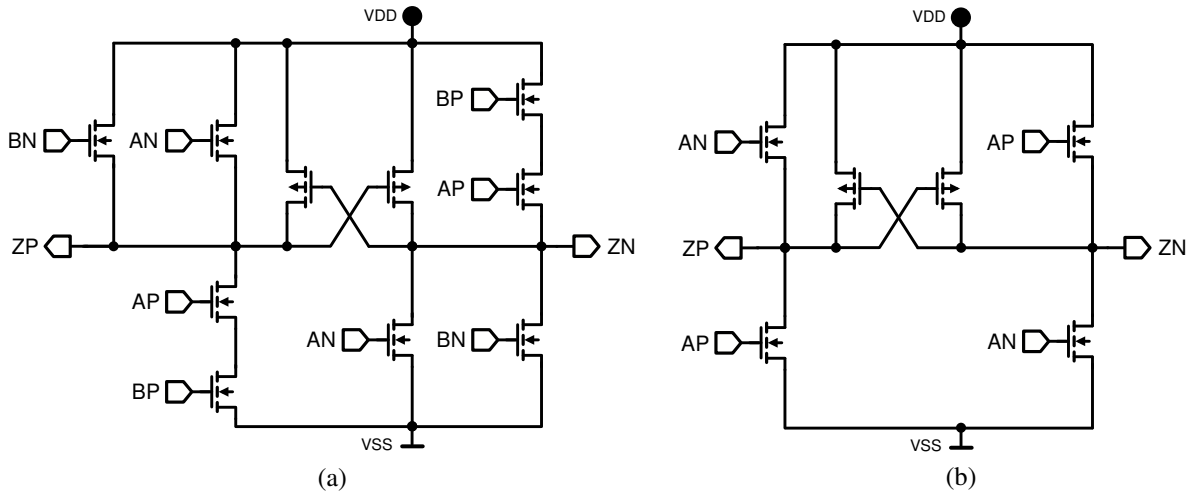


Figure 5.15: Circuit implementation of (a) – NAND gate and (b) – inverter used in phase-frequency detector

– reference frequency.

For $t_{lock} = 0.2$ ns and reference frequency of 64 MHz the duty cycle is $\delta_{lock} = 0.0128$.

When PLL operates in fractional-N mode the PFD output pulses width will not be constant as in the case of locked integer-N PLL, but will change from cycle to cycle depending on the sigma-delta modulator's control signal. Fig. 5.16 gives rather exaggerated illustration of PFD pulses in fractional-N mode.

Sigma-delta modulator generates digital sequence Y[n] with the average value

$$\overline{Y} = \frac{1}{N}\sum_{n=1}^{N} Y[n] \tag{5.9}$$

When instantaneous value of modulator's output exceeds the average value ($Y[n] > \overline{Y}$), than UPP pulse generated by the PFD will be wider, while DOWNP output will generate the pulse with a minimum width t_{lock}. Assuming that modulator changes the division ratio with a unity step, UPP pulse width excess defines as:

$$t_{sdm}[n] = \frac{\left|\overline{Y} - Y[n]\right|}{f_{out}}, \tag{5.10}$$

where f_{out} is the VCO output frequency.

For the case when $Y[n] < \overline{Y}$, UPP output generates a pulse with the width t_{lock}, and DOWNP produces a wider pulse defined by the same expression (5.10). For further charge pump noise analysis the instantaneous duty cycle excess of PFD pulses in fractional-N mode is defined:

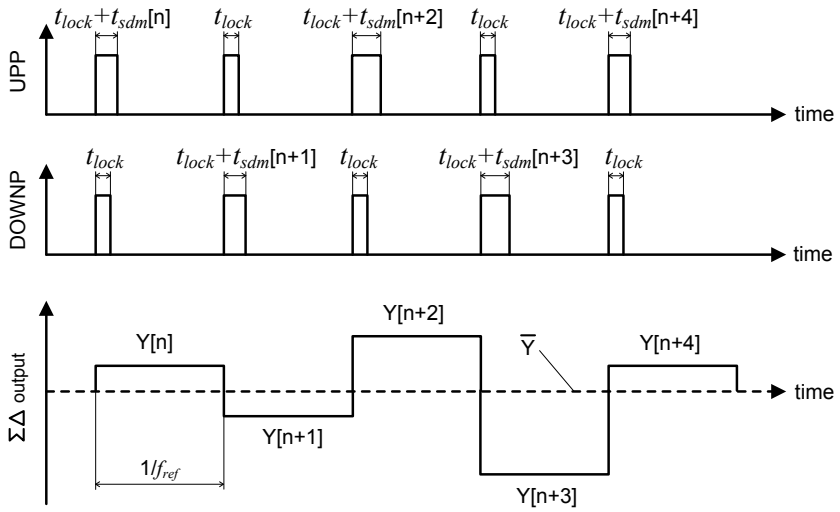


Figure 5.16: Phase-frequency detector output in fractional-N mode

$$\delta_{sdm}[n] = t_{sdm}[n] f_{ref} = \frac{f_{ref} \left| \overline{Y} - Y[n] \right|}{f_{out}} \tag{5.11}$$

The average duty cycle excess defines as

$$\overline{\delta_{sdm}} = \frac{1}{N} \sum_{n=1}^{N} \delta_{sdm}[n] \tag{5.12}$$

Simulated value for $\overline{\delta_{sdm}}$ is 0.006.

Special care is taken with the charge pump design to minimize the risk of significant reference spurious breakthrough caused by mismatches or leakage currents. In order to investigate parasitic influence of the integrated digital sigma-delta modulator on the PLL spurious performance, tones in the VCO spectrum caused by the charge pump imperfections must be well below the spurious provoked by substrate noise coming from the digital sigma-delta modulator. To meet such requirements high impedance current sources together with dynamic current matching are used. Charge pump is aimed to output currents in the range from 10 μA to 300 μA. Charge pump is driven directly by the phase-frequency detector.

Charge pump circuit diagram is shown in Fig. 5.17. Differential control terminals for the current switches (SNK and SRC) are connected directly with the differential output of the PFD: SRC with UP and SNK with DOWN. Current steering architecture provides high switching speed because the current sources ISRC_n and ISRC_p are always on. Complementary (NMOS in parallel with PMOS) current switches reduce the charge injection during the change in state of the charge pump. OpAmp-based voltage follower OP_1 tunes the voltage at charge pump

dummy current branch to be equal to the loop filter output voltage. This minimizes the charge sharing effect when current sources are connecting/disconnecting from the loop filter. The output voltage of the loop filter, which is low-pass filtered and much more smoothed than the voltage immediately after the charge pump, is used as the input for OP_1.

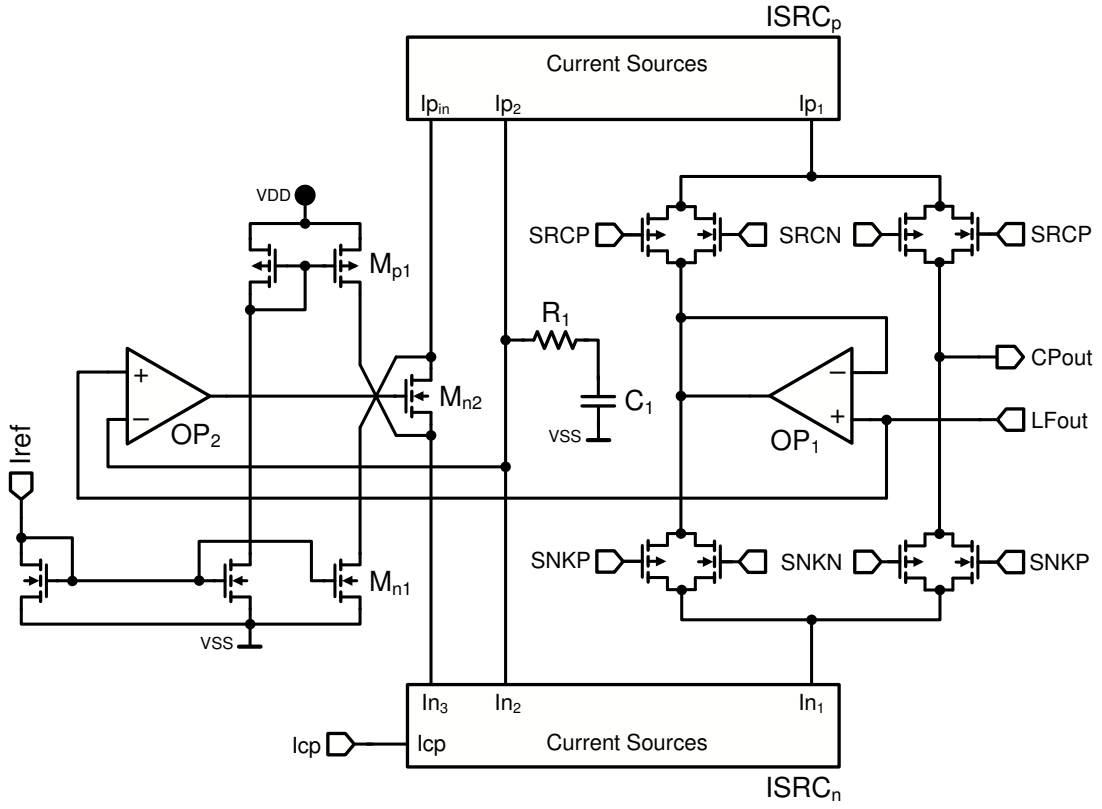


Figure 5.17: Charge pump circuit diagram

Säckinger (or regulated cascode) circuits offering high voltage swing and high output impedance are used as the current sources for the charge pump [Säckinger 90]. Even implemented in transistors with close to the minimum feature size, regulated cascode implementation still provides very high output impedance and noise contribution similar to that of simple cascode circuit having the same transistor size. Such features of regulated cascode current source make it an attractive choice for using in compact high performance integrated charge pump.

Fig. 5.18 illustrates schematic diagrams of sourcing ($ISRC_p$) and sinking ($ISRC_n$) current sources. To maximize the output voltage swing the circuits are implemented in low-V_t transistors. Both blocks contain two regulated cascode current sources: the first one provides the current for charge pump (outputs In_1 and Ip_1), the second one serves for precise matching of sourcing and sinking currents (outputs In_2 and Ip_2). Since all current sources are identical, the outlined current mirror in Fig. 5.18(a) is considered further for description.

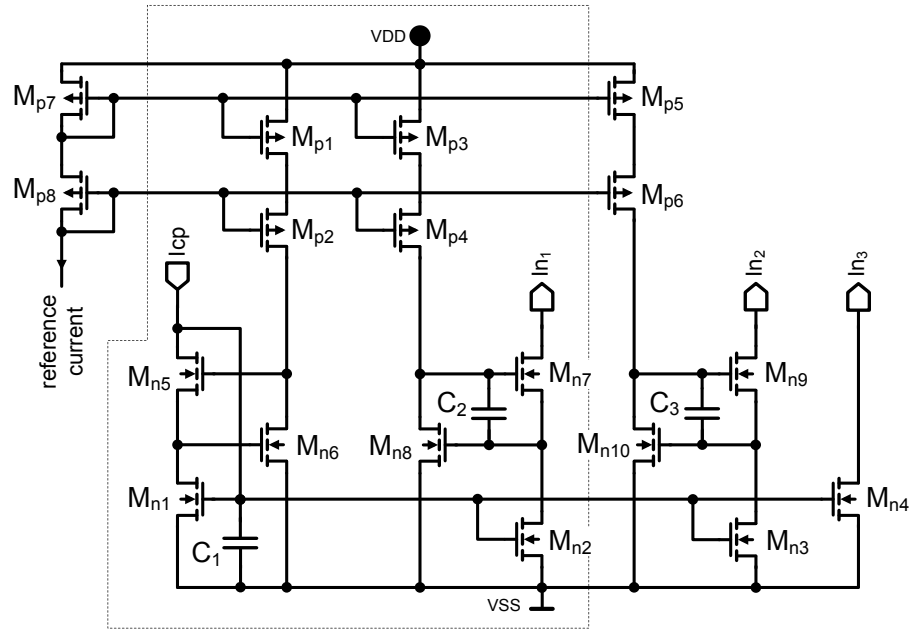
The current of regulated cascode circuits is mirrored from the diode-connected regulated cascode (transistors M_{n1}, M_{n5}, and M_{n6}). Gate-source voltage of M_{n2} defines the current flowing through the regulated cascode circuit. Capacitor C_1 realized as capacitively connected MOS transistor serves for quietening the control voltage of current sources, thus, stabilizing generated current. Feedback common source amplifier M_{n8} with active cascode load M_{p3} and M_{p4} keeps the drain-source voltage of current transistor M_{n2} stable.

Since regulated cascode current source is a circuit with a feedback, stability analysis is required to ensure that it is free of oscillation. Classical AC analysis of an open-loop circuit could be somewhat complicated and inaccurate for a current source operating in a nonlinear mode with wide output voltage swing. Thus, transient analysis was carried out to ensure stability of the regulated cascode current source under different operating conditions.

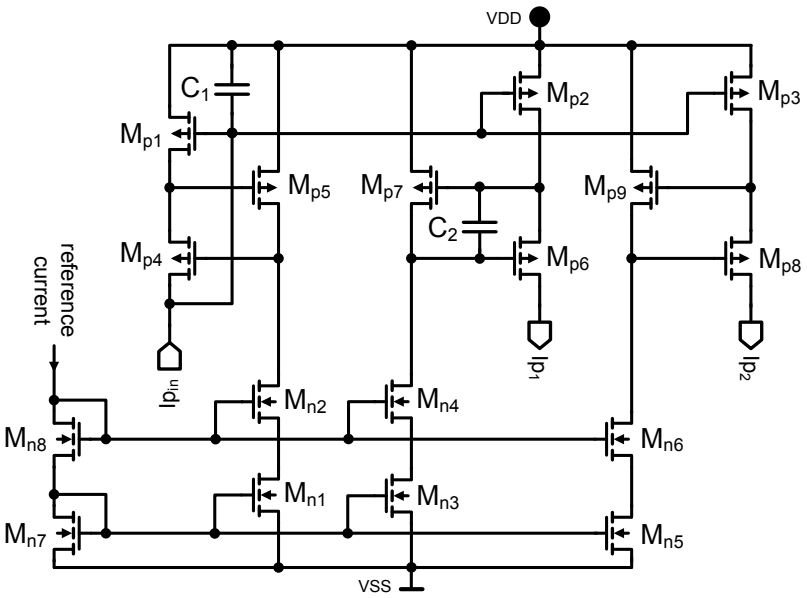
Uncompensated current source responses with dumped oscillation on the step voltage change. Since charge pump output voltage constantly experiences sharp voltage changes additional compensation is introduced into the circuit to avoid excessive ringing. Narrowbanding compensation method is realized by inserting capacitance C_2 between gates of cascode and amplifier transistors. C_2 is implemented as a capacitively-connected MOSFET. Diagrams obtained after the transient simulation of compensated and uncompensated regulated cascode current mirrors are illustrated in Fig. 5.19. As a stimulus step voltage changing from 0.6 V to 0.8 V was applied to the terminal In_1. The presence of compensated capacitance reduces current overshot and eliminates oscillation. Settling time, however, increased by more than four times. Simulation also reveals higher immunity of the compensated regulated cascode current source to the supply voltage perturbations.

Fig. 5.20 shows simulated DC transfer characteristics of the designed current sources. In Fig. 5.21 output resistance of the circuits operating with different output currents is demonstrated. The highest output resistance and voltage swing is obtained with the current of 15 μA. Operating with the nominal current of 100 μA charge pump could provide high output resistance (resulting in better linearity and current source matching) within around 50% of supply voltage range.

For better current source matching independently on the charge pump output voltage, sourcing current source is made tunable. The reference current coming out of the programmable current bank is applied to the $ISRC_n$ current mirror (terminal Icp). Transistor M_{n4} provides the current for $ISRC_p$ block. Because of relatively low output impedance of M_{n4}, its drain current can easily be tuned by changing the drain-source voltage (see Fig. 5.18(a)). Transistor M_{n2} in the charge pump in Fig. 5.17 performs this function. Controlled by the OpAmp OP_2, it regulates the current coming out of Ip_{in} is such a way that capacitor C_1 tends to have the same voltage as at the output of the loop filter, thus making the sourcing and sinking currents match each other. In order to make a feedback loop formed by the OpAmp and current sources stable, resistor R_1 is added is series



(a)



(b)

Figure 5.18: Circuit implementation of charge pump current sources: (a) – ISRC$_n$, (b) – ISRC$_p$

with the capacitance, introducing a pole to the loop and increasing the phase margin.

Additional current source made of M$_{n1}$ provides a current of 5 μA in order to avoid a theoretically possible unwanted latched state of charge pump when no

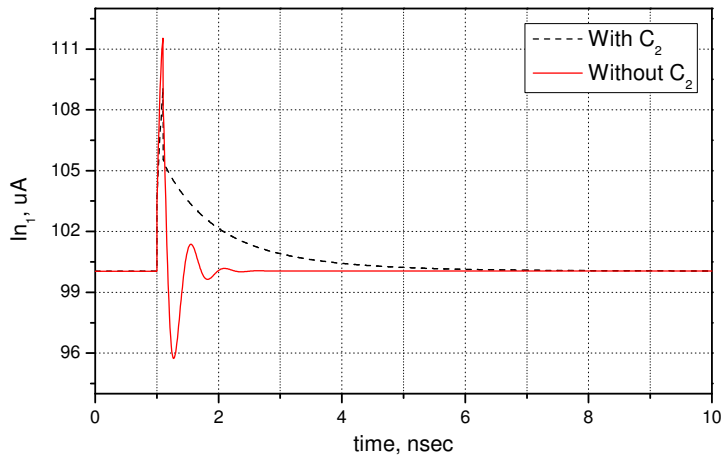


Figure 5.19: Transient response of the regulated cascode current source on the step output voltage change

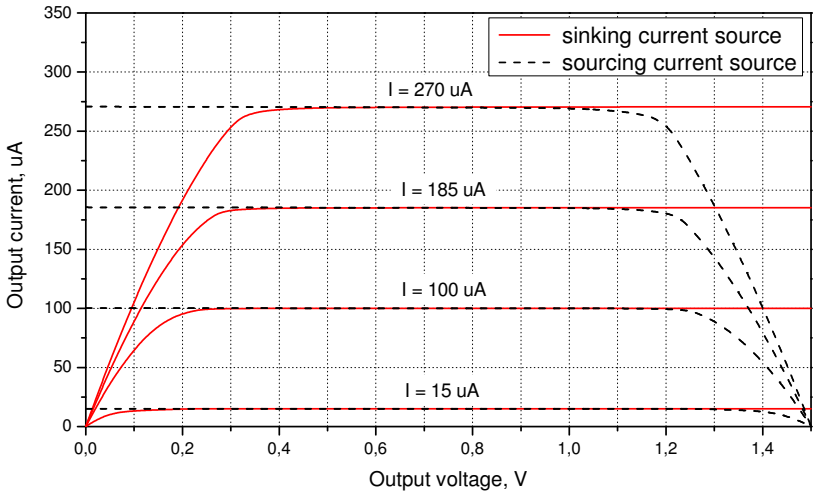


Figure 5.20: Simulated DC transfer characteristics of the current sources

current is flowing out of ISRC$_p$. PMOS transistor M$_{p1}$ compensates the current of M$_{n1}$. Moreover, both M$_{n1}$ and M$_{p1}$ speed-up the settling of the feedback during the significant change of charge pump current.

Finally, Fig. 5.22 shows simulated average mismatch current of charge pump in locked PLL depending on the output voltage and nominal charge pump current.

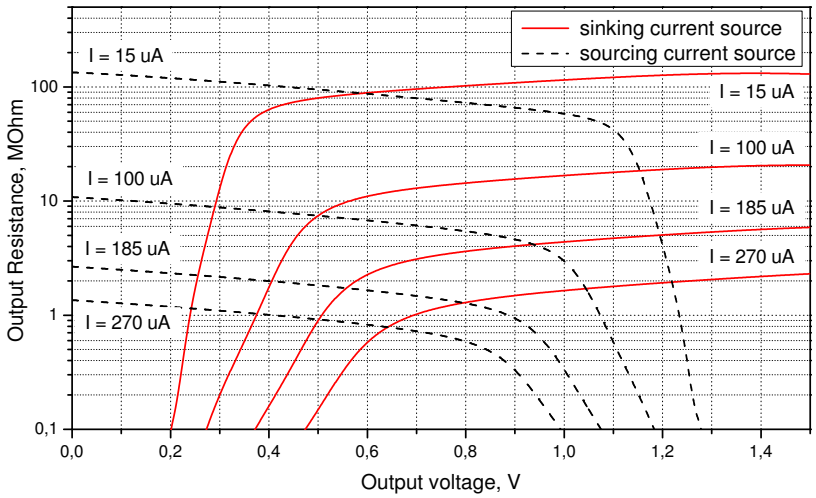


Figure 5.21: Simulated DC output resistance of the current sources

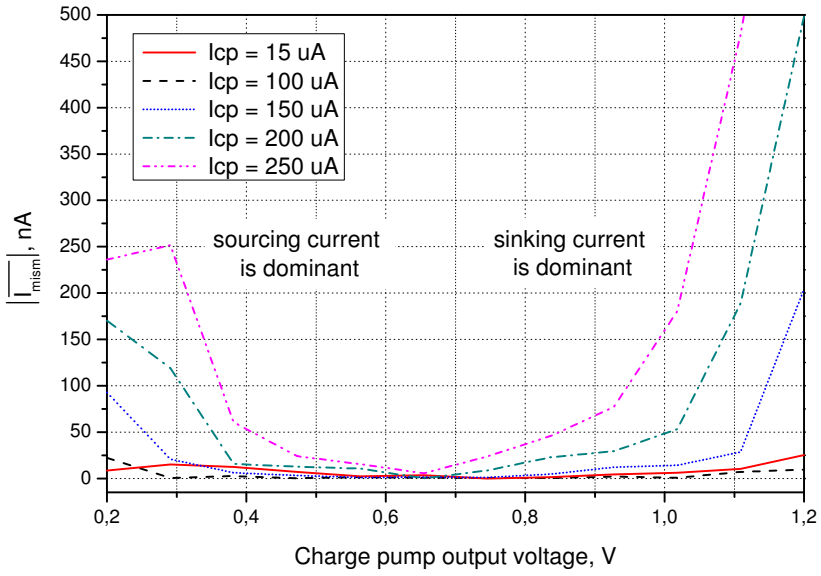


Figure 5.22: Simulated charge pump current mismatches

The difference between the currents of sinking and sourcing current sources is denoted as $I_{mism}(V_{CPout})$ and is a function of charge pump output voltage. When the loop is in-lock, meaning that the phase difference of the signals applied to

PFD equals zero, PFD generates both UP- and DOWN pulses 0.2 ns wide. During this time charge pump supplies mismatch current to the loop filter. The average mismatch current of the charge pump is defined as:

$$\overline{I_{mism}(V_{CPout})} = I_{mism}(V_{CPout})\delta_{lock}, \tag{5.13}$$

where δ_{lock}, defined by (5.8), is the duty cycle of charge pump output signal when the PLL is in-lock.

In Fig. 5.22 the absolute value of $\overline{I_{mism}(V_{CPout})}$ is shown. For the output voltages up to 0.65 V sourcing current source is dominant and $\overline{I_{mism}(V_{CPout})}$ is positive, while for the output voltages exceeding 0.65 V average mismatch current is negative. Charge pump demonstrates good current source matching operating with the nominal currents up to 150 μA.

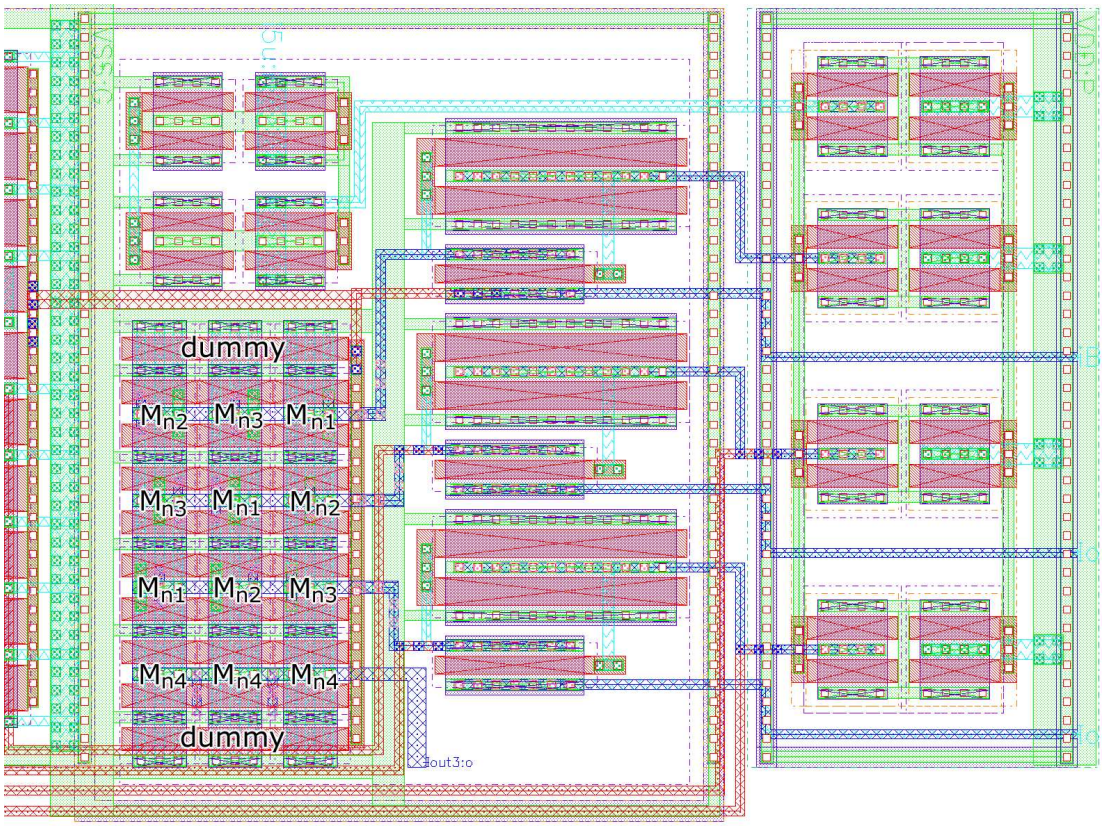


Figure 5.23: Layout of ISRC$_n$ block

In order to achieve predicted current matching, currents flowing into In$_1$ and In$_2$ terminals must be equal. The same condition must hold true for Ip$_1$ and Ip$_2$ terminals. Charge pump current is the most sensitive to mismatches in transistors M$_{n2}$ – M$_{n3}$ and M$_{p2}$ – M$_{p3}$ (see Fig. 5.18). Common-centroid layout technique

is used for compensating the influence of process variations on transistor matching [Hasting 01]. Fig. 5.23 illustrates the layout of sinking current source. Each transistor M_{n1}, M_{n2}, and M_{n3} consists of 3 parts compactly and symmetrically distributed over the area. At both sides dummy structures are placed to reduce the variations in edge transistors.

Noise Contribution

The noise source ϕ_{pd} in Fig. 5.2 represents the noise contribution of the phase-frequency detector and is assumed to be white. However, since differential realization of PFD demonstrates very good jitter characteristics, this noise source is well below the charge pump noise, therefore it could be neglected:

$$\phi_{pd} \;=\; 0\ rad/\sqrt{Hz} \tag{5.14}$$

The charge pump noise distribution over the frequency is substantially defined by the noise properties of the current sources ISRC_n and ISRC_p and duty cycle of the UP-DOWN pulses of the locked PLL. Indeed, charge pump current noise flows to the output only during the fraction of time when UP and DOWN outputs of the PFD are active. Such assumption is proved by the simulations carried out in [Perrott 97]. This results in the following expression for the charge pump noise power spectral density:

$$i_{cp}^2 = (i_{src_p}^2 + i_{src_n}^2)\delta_{lock} = i_{src}^2\delta_{lock}, \tag{5.15}$$

where $i_{src_p}^2$ and $i_{src_n}^2$ are the power spectral densities of the noise generated by the ISRC_n and ISRC_p blocks respectively, and δ_{lock} is a duty cycle defined by (5.8).

It is assumed that noises of the sinking and sourcing current sources are not correlated. The charge pump noise variations due to the noise in current source matching circuitry (output In_3 of ISRC_n) are omitted.

The noise performance of regulated cascode current source is very similar to the simple cascode circuit [Säckinger 90]. In ISRC_n the main contribution comes from transistor M_{n2} (see Fig. 5.18). The dominant noise sources for MOSFET in the saturation (active) region are flicker and thermal noise [Johns 97]. Flicker noise corner frequency for modern integrated MOS transistors can reach the values of several megahertz, which is close (or at least comparable) to the PLL bandwidth. Since charge pump noise is not suppressed by the PLL at frequency offsets below the bandwidth, flicker noise of the current sources can contribute significant fraction into the total noise of the PLL.

The noise performance of regulated cascode current source can hardly be predicted analytically since it depends not only on the realization of the current mirror, but also on the noise characteristics of the reference source applied to the current mirror. The strongest influence of the reference source happens at

low frequencies, namely where flicker noise is dominant. Thus, the whole reference chain (which practically can contain several current sources) must be taken into account. For this reason the noise performance of the charge pump current sources was estimated by means of simulation.

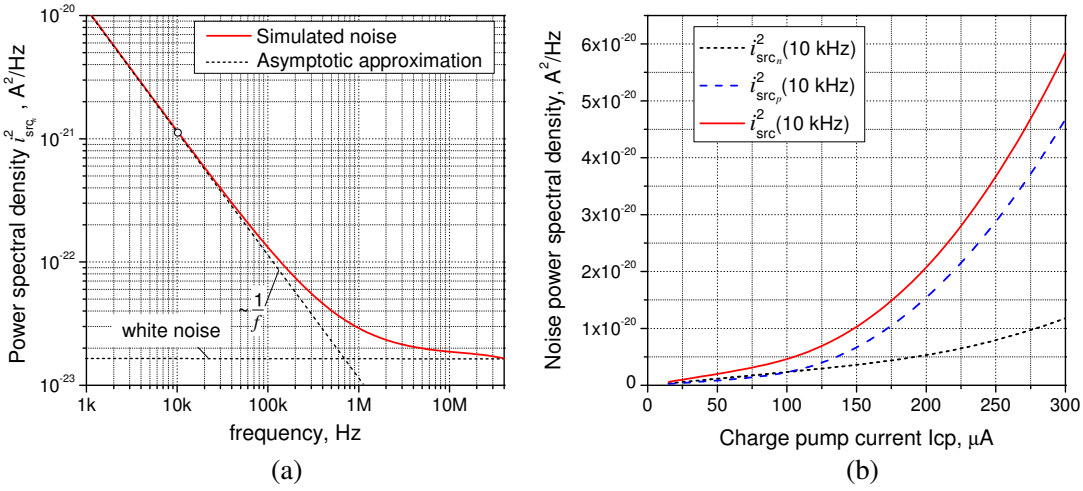


Figure 5.24: (a) – noise power spectral density of the sinking current source for output current of I_{cp} = 50 μA, (b) – noise power spectral densities at 10 kHz versus charge pump output current

The simulated noise power spectral density of $ISRC_n$ current source for output current of 50 μA is shown in Fig. 5.24(a). It can be approximated by the following function:

$$i^2_{src_n}(f) \approx \frac{i^2_{src_n}(10\ kHz) \cdot 10\ kHz}{f} + i^2_{nf.src_n}, \tag{5.16}$$

where $i^2_{src_n}(10\ kHz) = 1.16 \cdot 10^{-21}$ A^2/Hz is a simulated noise power spectral density at 10 kHz, and $i^2_{nf.src_n} = 1.65 \cdot 10^{-23}$ A^2/Hz is a noise floor.

Flicker noise corner frequency is 700 kHz. Similar noise distribution demonstrates sourcing current source. The noise of the current source strongly depends on the output current I_{cp}. Fig. 5.24(b) shows the noise power spectral density at 10 kHz versus DC current of $ISRC_n$, $ISRC_p$, and both of them.

The total power spectral density of the noise contributed by charge pump in locked PLL operating in integer-N mode is

$$i^2_{cp}(f, I_{cp}) \approx \left(\frac{i^2_{src}(10\ kHz, I_{cp}) \cdot 10\ kHz}{f} + i^2_{nf.src} \right) \delta_{lock}, \tag{5.17}$$

where $i^2_{nf.src}$ is a noise floor of a total noise coming from ISRC_n and ISRC_p sources. Although it is also dependent on the output current, here it assumed to be constant since at frequency offsets exceeding PLL bandwidth it is well below the noise of the voltage-controlled oscillator. The simulated numerical value of the noise floor is $i^2_{nf.src} = 2.5 \cdot 10^{-23}$ A^2/Hz.

The noise of both current sources at 10 kHz offset can be approximated by the simple quadratic function to be easily used for further PLL noise simulation:

$$i^2_{src}(10\ kHz, I_{cp}) \approx (g \cdot I_{cp} + i_o)^2\,, \tag{5.18}$$

where the parameters values should be $g = 7.26 \cdot 10^{-7}$ $1/\sqrt{Hz}$ and $i_o = 9.11 \cdot 10^{-12}$ $\text{A}/\sqrt{Hz}$ to get the same curve as shown in Fig. 5.24(b).

Finally, substituting (5.18) into (5.17) results in charge pump noise root spectral density which can be used directly in the PLL linear model (integer-N mode of operation is assumed):

$$i_{cp}(f, I_{cp}) \approx \sqrt{\left(\frac{(g \cdot I_{cp} + i_o)^2 \cdot 10\ kHz}{f} + i^2_{nf.src}\right)\delta_{lock}} \tag{5.19}$$

Since charge pump noise depends on the duty cycle of current pulses, expression (5.19) must be corrected before modeling the noise of PLL operating in fractional-N mode. The width of current pulses in the PLL operating in fractional-N mode constantly changes from cycle to cycle. The behavior of pulses in a graphical way is demonstrated in Fig. 5.16. After correction, (5.19) transforms into

$$i_{cp}(f, I_{cp}) \approx \sqrt{\left(\frac{(g \cdot I_{cp} + i_o)^2 \cdot 10\ kHz}{f} + i^2_{nf.src}\right)(\delta_{lock} + \delta_{sdm})}, \tag{5.20}$$

where $\overline{\delta_{sdm}}$ is given by (5.12).

5.3.3 Frequency Divider

According to initial specifications, PLL should be synchronized by the reference frequency of 50 MHz because oscillators with such frequency are widely available on the market. In order to generate carrier frequency in 11 GHz range, division ratio should lie in the vicinity of 220. During the design of prescaler, frequency division ratio range was considerably extended without any significant increase of prescaler's complexity. Division ratio range extends from 41 to 276 with the step of 1 allowing the PLL to be synchronized by any reference in the range 39 MHz – 273 MHz to provide locking within the whole VCO tuning range.

Block diagram of the frequency divider chain is presented in Fig. 5.25. It is based on the phase-switching prescaler proposed in [Craninckx 96]. With this architecture unity-step frequency division can be realized in low-speed CMOS logic together with a couple of fast D-flip-flops. The first two high frequency dividers DIV_1 and DIV_2 scale down the VCO frequency by the factor of 4. Since compact static CMOS flip-flops cannot operate at frequency as high as 11 GHz, current-mode logic (CML) dividers are used to decrease the frequency to 2.75 GHz. The latter stages are implemented in CMOS logic. The divider DIV_2 outputs four phases which are applied to the phase selector. After phase selector PS_1 and divide-by-2 circuit DIV_3 the signal is applied to the DX_1 block of the divider chain, which performs a final frequency division. The last stage operates at 1.4 GHz.

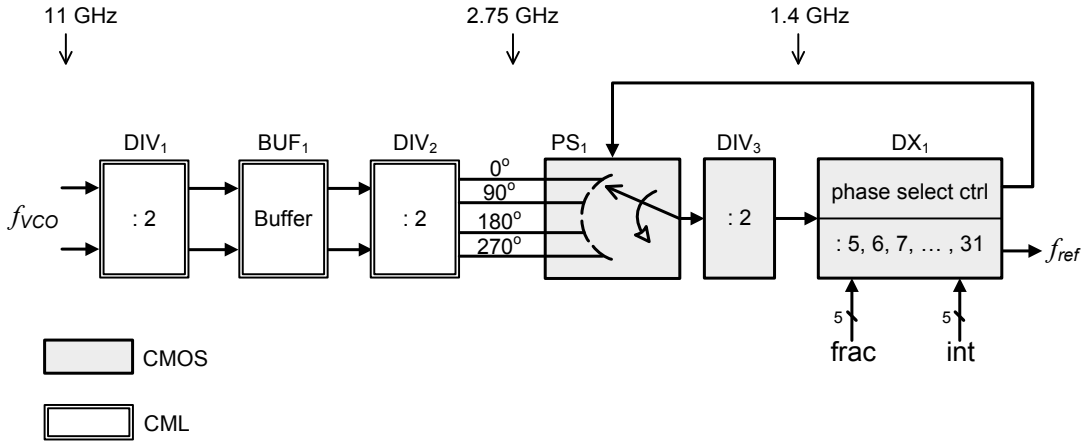


Figure 5.25: Frequency divider block diagram

The circuit diagram of high-frequency divider is shown in Fig. 5.26. It consists of a D-flip-flop comprising a feedback loop. D-flip-flop in turn consists of two master-slave latches working as current switches. Fully, differential, all NMOS design provides switching speed sufficient for dividing the VCO output signal.

The current for latches is provided by the stacked current sources made of regular- and low-V_t transistor. The latter operates as a cascode transistor, gates of both transistors are connected together. Such current source configuration implemented in Infineon C11RF technology provides the output impedance above 1 kΩ within the operating conditions of the latch [Kehrer 03]. DC tail current flowing through one current source is $I_{DC} = 7.5$ mA. Loaded by the resistors R = 120 Ω each latch ideally should provide a differential output voltage swing of $I_{DC} \cdot R = 0.9$ V. Simulations, however, showed slightly lower value caused by the influence of parasitic capacitances of transistors.

Divider generates four-phases output. For correct operation of phase-switching prescaler the phase shift generated by the divider must be negative, namely, Q90 output lags the Q0 by 90 degrees, Q180 lags the Q90 by 90 degrees and so on.

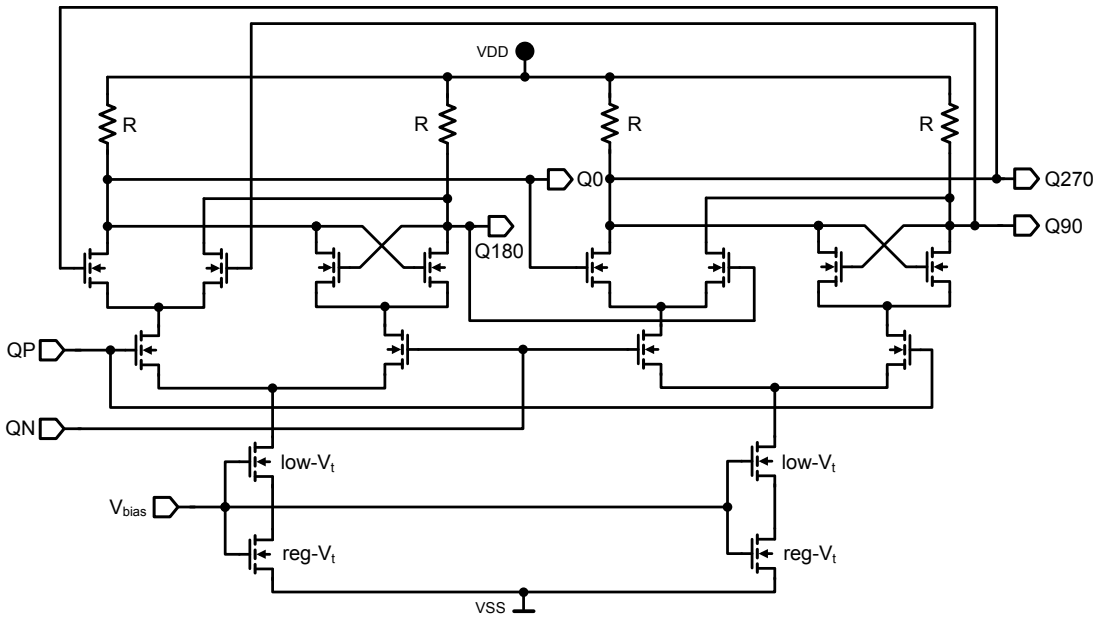


Figure 5.26: Current mode logic divide-by-2 circuit

Circuit diagram of the buffer placed between the first and the second CML dividers is shown in Fig. 5.27. Its role is two-fold: it provides interstage DC level shift and is also able to drive mixer of the receiver integrated on the same die. DC level shift is performed by the common-mode resistor R_1 having the nominal value of 20 Ω. With the DC current of 7.5 mA flowing across the buffer the peak value of the output voltage is shifted down by 0.15 V. Output voltage swing determined by the load resistors $R_2 = R_3 = 110$ Ω equals 0.82 V.

Since each high-frequency divide-by-2 circuit comprises two current sources providing the current of 7.5 mA, the whole CML chain, together with the interstage buffer, consumes 37.5 mA, which is almost 2/3 of the whole current consumed by the PLL.

After the frequency is scaled down to 2.75 GHz it is applied to the phase selector. With the help of a phase selector total division ratio can be changed with the unity step with the ratio equals to the period of reference signal. The block diagram of the phase selector is presented in Fig. 5.28.

Input buffer BUF shown in Fig. 5.29(a) transforms the signal after CML divider into the full-swing digital signal necessary for CMOS logic. It is DC decoupled from the divider, voltage level transformation performs an inverter M_{n2}–M_{p2} which operates as a high-gain voltage amplifier. An operating point is set by transistors M_{n1} and M_{p1} which are connected as diodes. The sizes of M_{n1} and M_{p1} are the same as of M_{n2} and M_{p2}, thus biasing voltage drives both M_{n2} and M_{p2} into saturation region, offering the highest gain at such operating conditions.

Capacitor C_b is implemented as a vertical parallel plates structure [Aparicio 02].

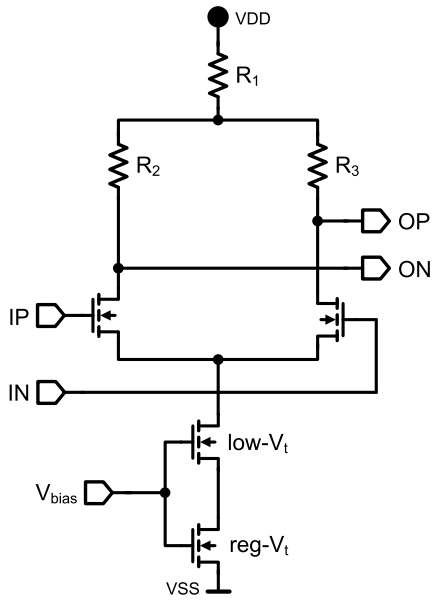


Figure 5.27: Buffer circuit diagram

Fig. 5.29(b) demonstrates the view on the vertical parallel plates capacitor layout. Among the advantages of such structure are high capacitance per unit volume, low parasitic capacitance to the substrate and geometrical symmetry of the structure (resulting in equal parasitic capacitances to the substrate and equal series resistance for both plates). The structure is implemented in three metallization layers drawn at minimum design rule width and space. Each plate is composed of 20 fingers (just 3 of them are shown in the picture).

The value of the capacitor can be approximated as:

$$C_b = \frac{\epsilon_d \epsilon_0}{L_F} \cdot W_F H(2N_F - 1), \tag{5.21}$$

where ϵ_d is the relative permittivity of an insulator, ϵ_0 is the permittivity of free space, L_F – distance between the fingers (plates), W_F – width of the fingers, H – height of capacitor's plate, N_F – number of fingers in each plate.

The estimated capacitance of the implemented 20 fingers structure with $W_F = 8$ μm and $L_F = 0.2$ μm is 120 fF. Each plate has around 6 fF parasitic capacitance to the substrate.

All D-flip-flops in Fig. 5.28 are similar, implementation details are shown in Fig. 4.9.

The phase selector operates sequentially, picking up one input phase and connecting it to the output until the triggering signal appears at the control input phase_sel. When this happens, phase selector picks up another phase, which is 90 degrees lag to the currently selected phase. Each new phase selection results in an

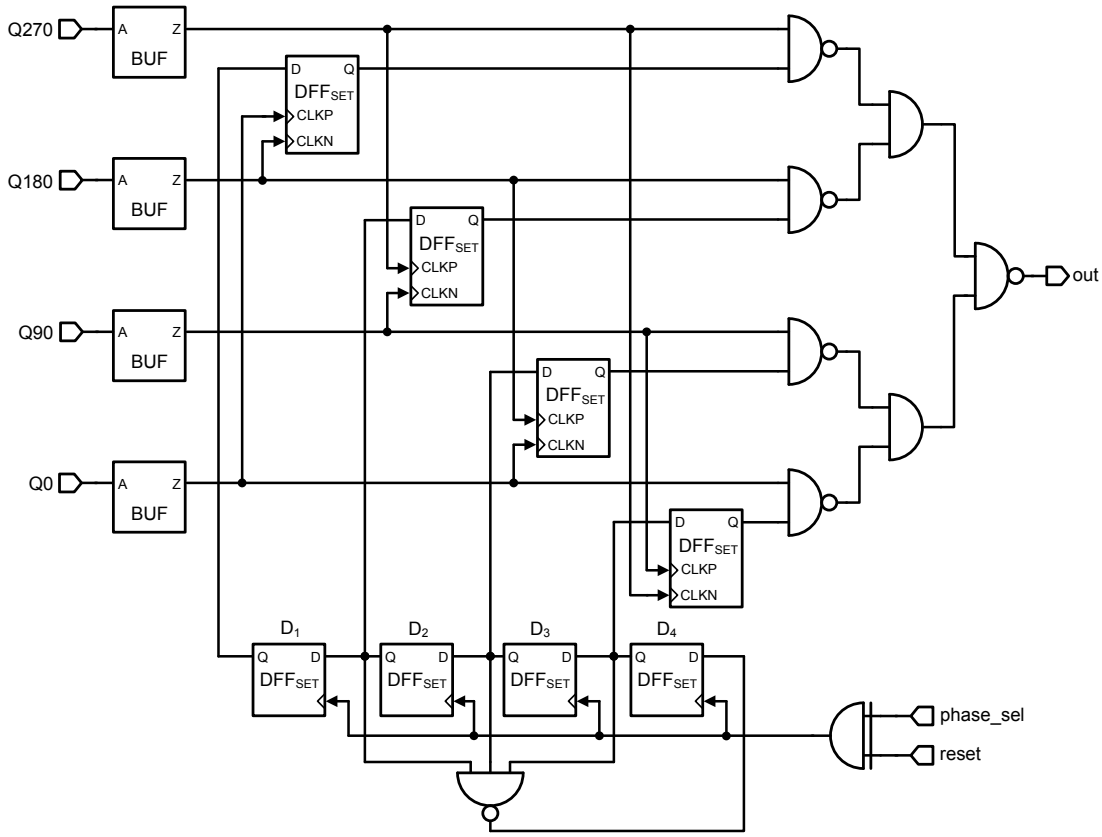


Figure 5.28: Phase selector diagram

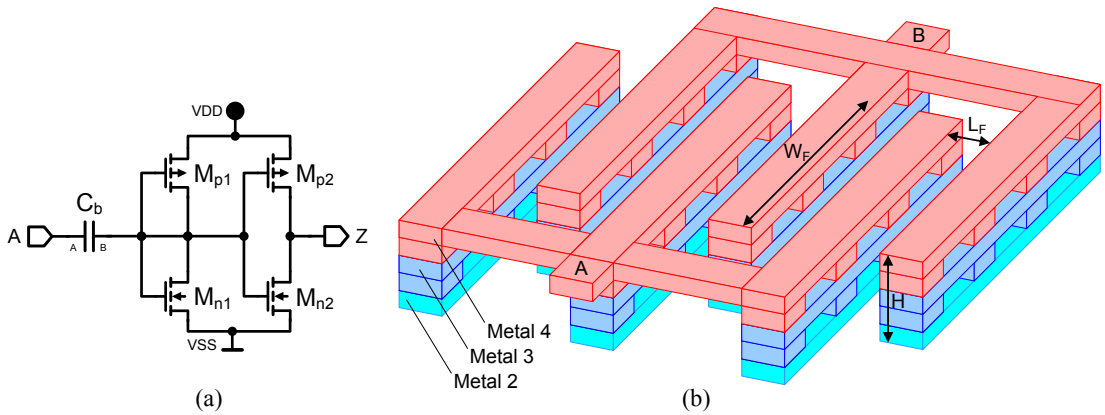


Figure 5.29: (a) – circuit implementation of the BUF block in Fig. 5.28, (b) – view on the layout of capacitor C_b

overall division ratio change by +1. Triggering signal is generated by the phase selector controller DX_1 and does not appear more often as once in two periods of phase selector's output signal.

The signal for phase_sel port cannot be generated until some periodic signal appears at the output of phase selector to trigger the phase selector controller. Such latched state can happen at start-up when at the outputs of D_1, D_2, D_3, and D_4 simultaneously appears logical '0'. Thus, reset input is introduced to the phase selector serving for starting-up the circuit when latched state occurs. Circuit which generates the signal for reset port is demonstrated in Appendix A.2.

DX_1 is an essential part of the divider performing the final frequency division and generating triggering signal for the phase selector. It is controlled by two 5-bit digital words int and frac. frac defines the number of triggering pulses generated by the phase selector controller during one reference cycle. It can be changed with a reference frequency rate and is used for implementing fractional division. Sigma-delta modulator's output sequence is applied to the three least significant bits of frac input. The rest two bits are controlled statically. Int serves for setting division modulus offset and is intended to be static signal. A detailed circuit diagram of DX_1 together with the description are given in Appendix A.1.

The overall division ratio of the divider shown in Fig. 5.25 defines as:

$$N = \frac{f_{VCO}}{f_{ref}} = 8 \cdot int + frac, \tag{5.22}$$

where

$$int = \sum_{i=0}^{4} 2^i \cdot int_i; \tag{5.23}$$

$$frac = \sum_{i=0}^{4} 2^i \cdot frac_i. \tag{5.24}$$

In (5.23) and (5.24) $int_i \in \{0; 1\}$ and $frac_i \in \{0; 1\}$ represent i-th bit of the digital words int and frac respectively. The factor 8 in (5.22) is due to the three divide-by-2 stages DIV_1, DIV_2 and DIV_3.

The allowable range for control words are (decimal values):

$$int \in \{5, ..., 31\} \tag{5.25}$$

$$frac \in \{1, ..., int - 4\} \tag{5.26}$$

Both ranges are limited by the words resolution and specific hardware realization of DX_1. More detailed description is presented in Appendix A.1.

Using (5.22) and taking into account (5.25) and (5.26) division ratio range can be estimated (within this range division ratio can be changed with a unity step):

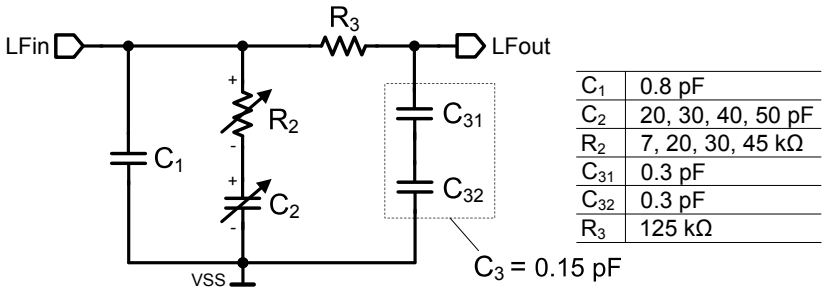
$$N \in \{41, ..., 275\} \tag{5.27}$$

The whole frequency divider occupies a silicon area of 230 μm $\times$ 105 μm.

5.3.4 Loop Filter

The circuit diagram of the implemented third order passive loop filter is shown in Fig. 5.30. Capacitor C_2 and resistor R_2 are made tunable, since their values have the strongest impact on the filter transfer function. Fig. 5.31 and Fig. 5.32 demonstrate the circuit implementation of R_2 and C_2. Small blocking capacitors C_b with the nominal of 80 fF in the tunable capacitor C_2 serve for suppressing any voltage variation at the gate terminals of transistors.

The values for the loop filter components were determined numerically by means of behavioral model simulation.



C_1	0.8 pF
C_2	20, 30, 40, 50 pF
R_2	7, 20, 30, 45 kΩ
C_{31}	0.3 pF
C_{32}	0.3 pF
R_3	125 kΩ

Figure 5.30: Loop filter circuit diagram

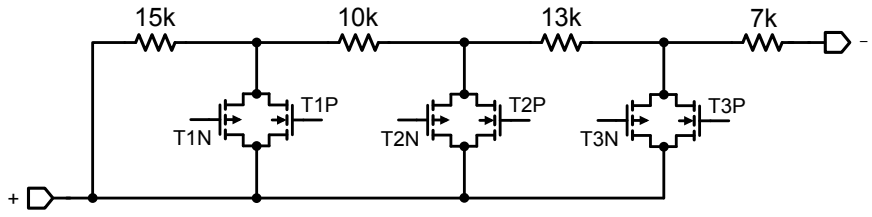


Figure 5.31: Implementation of the tunable resistor R_2 in loop filter

Special care has been devoted to the layout design of the loop filter. All capacitors (except C_b) of loop filter are implemented as the thin-film MIM capacitors. This capacitor type is highly linear, has high accuracy, tight tolerance, and highest capacitance per unit area. The last feature is very important for implementing C_2, since 50 pF can occupy significant part of the silicon area (in the implemented filter it occupies the area of 220 μm $\times$ 115 μm). Moreover, MIM capacitors in C11RF technology are made of upper metallization layers which makes C_2 less

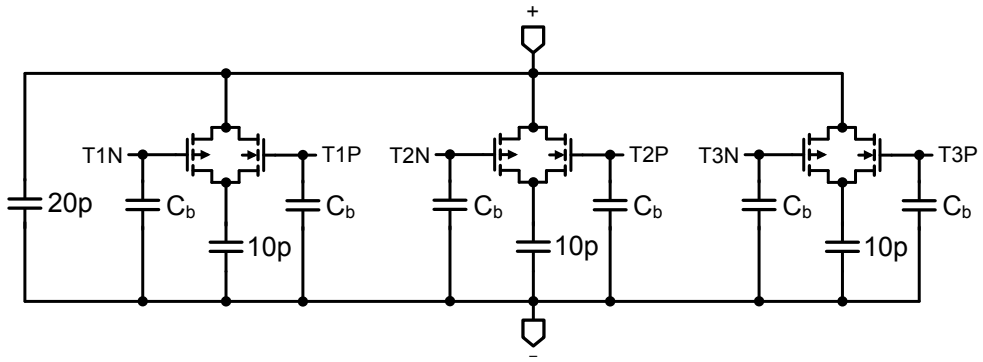


Figure 5.32: Implementation of the tunable capacitor C_2 in loop filter

sensitive to the switching noise coupled from the substrate. To protect further C_2 from the parasitic noise coupling it is placed above the n-well, which forms additional capacitive path from the substrate to the ground plate of C_2. N-well is connected to the ground terminal of the loop filter.

The layout dimensions of capacitor $C_3 = 0.15$ pF is relatively small, which makes it very sensitive to geometrical variations. To make it less sensitive to such variations C_3 is formed by C_{31} and C_{32} connected in series. The nominal capacitance of C_{31} and C_{32} is twice the capacitance of C_3, so are the dimensions.

Resistors R_2 and R_3 are realized in p^+ polysilicon with blocked salicidation which offers a reasonable tradeoff between the sheet resistance (resulting in an occupied area) and the tolerance. The width of R_2 is higher than of R_3 in order to decrease the sensitivity to geometrical variations.

Loop filter is placed as close to the VCO as possible. This is done to minimize the resistance between the VCO and loop filter grounds. Since the VCO frequency is dependent on the voltage between V_{tune} and VSS terminals (see Fig. 5.8) any noise at ground terminal of the loop filter with the presence of resistive path between the VCO and filter grounds will cause unwanted phase modulation of the oscillator's signal. However, when the VCO and filter ground terminals are connected together by the low-ohmic path the undesired substrate-to-phase noise transformation will be minimized.

Noise Contribution

There are two sources of noise in the loop filter: white thermal noise of resistors R_2 and R_3. The root spectral density of the voltage noise sources of resistors normalized to 1 Hz bandwidth are [Johns 97]:

$$v_{n.R2} = \sqrt{4kTR_2} \tag{5.28}$$

$$v_{n.R3} = \sqrt{4kTR_3} \tag{5.29}$$

for R_2 and R_3 correspondingly.

5.3.5 Reference Source

Reference source phase noise dominates in the overall PLL noise at low frequency offsets. Most of the PLL measurements were carried out using standard 64 MHz quartz oscillator (XO). For some measurements PLL was synchronized by 50 MHz quartz oscillator. The single-ended signal of the reference oscillator was transformed to the differential by means of an external coupler. The carrier power after the oscillator is 1.8 dBm. After the transformation to differential form each output delivers –1.2 dBm to the PLL, which results in 0.55 V peak-to-peak signal in 50 Ω load.

Fig. 5.33 illustrates the measured phase noise of the 64 MHz crystal oscillator. At frequency offsets below 1 MHz the curve exhibits a roll-off slope of –10 dB/dec. For the use in linear phase-domain model the XO noise is approximated by the following function:

$$\phi_{ref}(\Delta f) \approx \sqrt{2 \cdot \left(10^{\frac{\mathcal{L}_0}{10}} + 10^{\frac{\mathcal{L}_{b1}(\Delta f)}{10}}\right)} \tag{5.30}$$

where

$$\mathcal{L}_{b1}(\Delta f) = \mathcal{L}_1 + 10 \log \frac{\Delta f_1}{\Delta f} \tag{5.31}$$

Parameters used in (5.30) and (5.31) have the following values taken from the measured phase noise curve: $\mathcal{L}_1 = -130$ dBc/Hz, $\Delta f_1 = 10$ kHz, $\mathcal{L}_0 = -150$ dBc/Hz.

The proper design of input reference buffer is necessary for minimizing the degradation of reference source phase noise while delivering its signal to the phase-frequency detector. The buffer circuit implementation is demonstrated in Fig. 5.34. The differential interface is chosen for the reason of high common mode noise rejection ratio. The input signal is applied first to the differential preamplifier which drives the second high-gain stage. The second stage generates the sharp-slope signal spreading from VSS to VDD. Before applying to the phase-frequency detector, the signal for the reference buffer goes to the inverter implemented in PPCL logic (see Fig. 5.15(b) for implementation details).

5.4 Full PLL Layout

The full PLL layout including test pads is shown in Fig. 5.35. Special care is taken with placing switching noise sources and sensitive noise receptors. Since

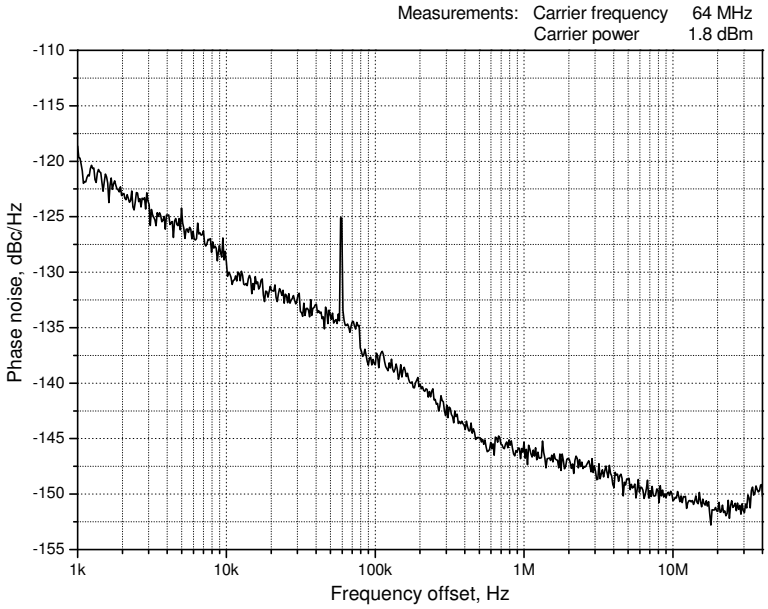


Figure 5.33: Measured phase noise of the 64 MHz quartz oscillator

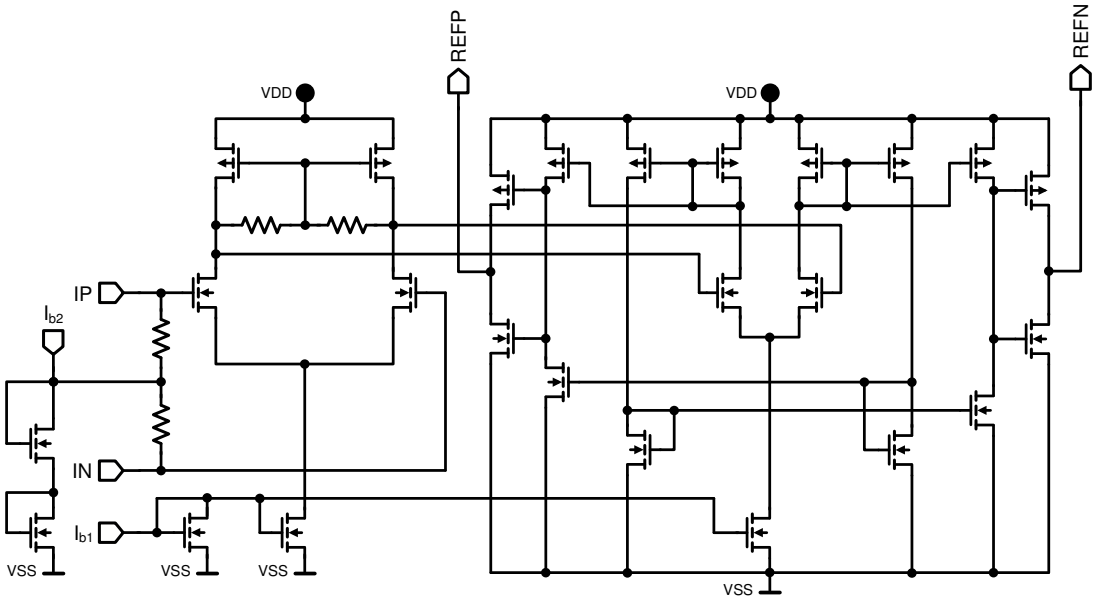


Figure 5.34: Input reference buffer circuit diagram

fabricated technology features non-epitaxial high resistive substrate, the amount of noise coupling can be reduced by increasing the separation distance between digital and analog blocks. The distance is, however, limited by the area required

for implementing blocks in layout. The use of extra silicon just for increasing the length of coupling path is not cost efficient solution.

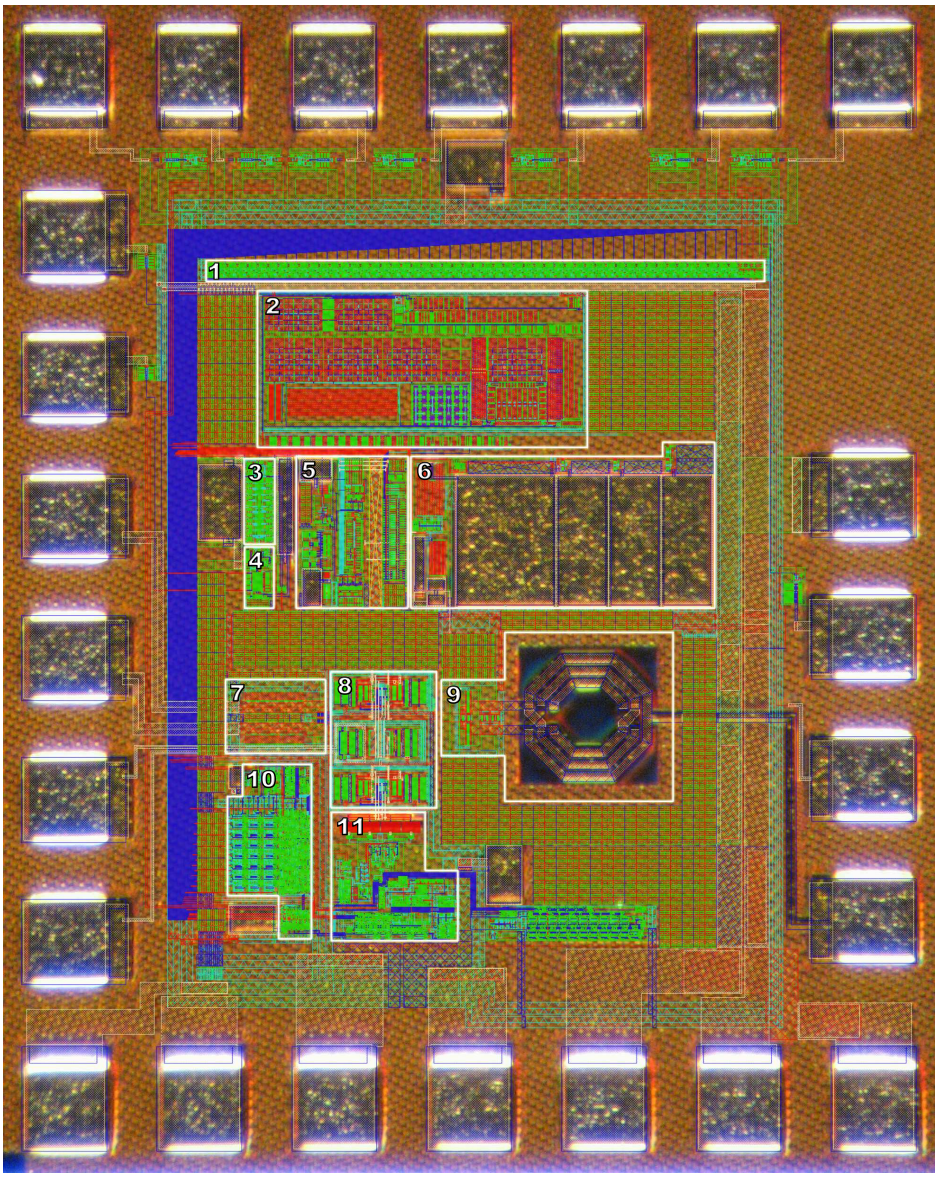


Figure 5.35: Chip layout. Blocks numeration: 1 – programmable register, 2 – bandgap reference, 3 – PFD, 4 – reference buffer, 5 – charge pump, 6 – loop filter, 7 – 11 GHz pad driver, 8 – CML divider and 5.5 GHz pad driver, 9 – VCO, 10 – sigma-delta modulator, 11 – CMOS divider

The main sources of noise are digital sigma-delta modulator and the part of the frequency divider implemented in CMOS logic (numbered as 10 and 11 in the figure). They are placed on the lower left corner as far as possible from the noise sensitive receptors. The VCO, the charge pump, and the loop filter belong to the noise sensitive receptors. Bandgap current reference supplies current for most of

the PLL blocks, thus the noise coupled into it can spread over the whole device. Thus, it is placed at the highest possible distance from the divider and sigma-delta modulator. The CML part of the divider is placed next to the VCO since it does not generate severe switching noise.

The guard rings were extensively used in layout of analog blocks. On one hand they reduce the risk of latch-up, on the other serve as a blocking feature for digital noise.

PLL incorporates three different supply networks: for analog blocks, for CML logic, and for CMOS logic. The supply nodes of all analog blocks are sufficiently blocked by on-chip PMOS capacitors (parts of the chip not surrounded by the white lines). Digital circuitry also incorporates blocking, but MIM capacitors instead of PMOS are used. This is done to minimize the coupling of the switching noise to the substrate, coming from the blocking capacitors.

The technology features a possibility to place a moat layer to break the conductive path formed by p-well between different regions of the substrate. Previous experience in this technology showed that moat does not decrease significantly the amount of coupled noise, while consuming relatively large die area – the minimum stripe width should be 10 μm. For this reason PMOS blocking capacitors placed in n-well are used as a physical barrier between analog and digital parts of the chip. By proper floorplanning n-well replaces the resistive path by the capacitive path at the surface of silicon substrate.

As it was demonstrated in Section 3.1, capacitive coupling between switching and sensitive interconnection lines can degrade the spurious performance of the PLL. The design is layed out in such a way that switching nodes do not intersect with sensitive analog wires. The line connecting the loop filter with a VCO is made as short as possible and is isolated from the digital wires. The feedback path connecting frequency divider with the phase-frequency detector (which is as long as 270 μm in the designed layout) is made differential to make it insensitive to the common-mode noise influence.

Chapter 6

Experimental Results

6.1 Fully Integrated 11 GHz Sigma-Delta PLL

The designed 11 GHz sigma-delta phase-locked loop with an ability to connect externally generated 3-bit bitstream for prescaler division ratio control was fabricated in 0.13 μm CMOS technology. The device is programmed by means of a 52-bit JTAG register. Generated differential LO signal at 11 GHz is routed to the output. The block diagram of the device is shown in Fig. 6.1.

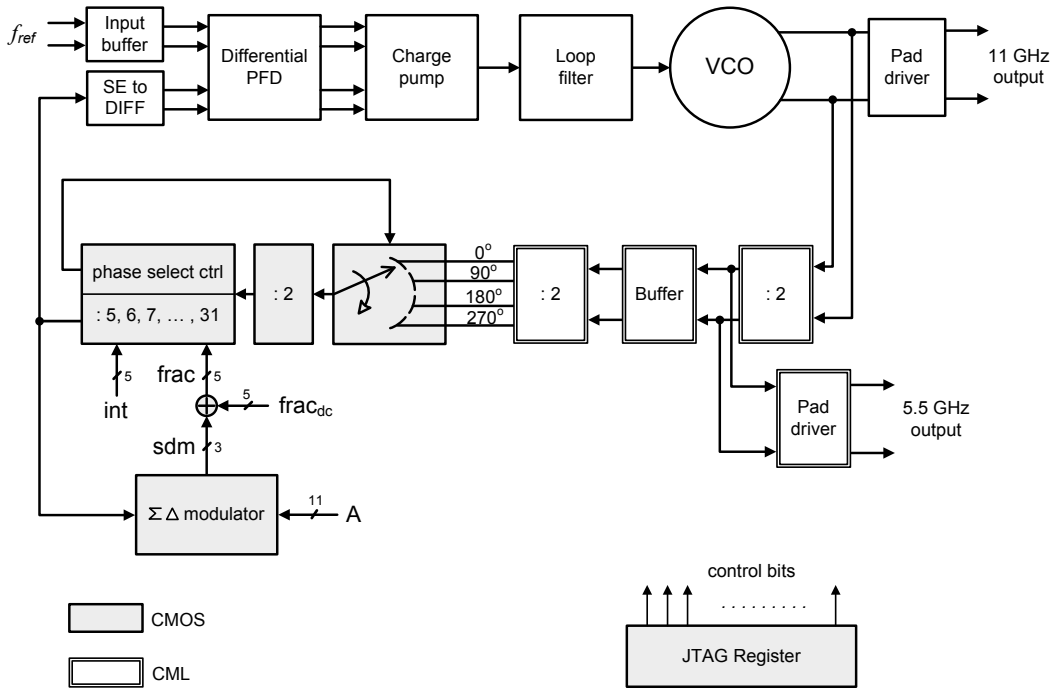


Figure 6.1: Block diagram of the PLL

The device comprises on-chip sigma-delta modulator implemented as a MASH 1-1-1

structure in a dual edge triggered style. The resolution of each accumulator is 14 bits. The 11 most significant bits are used for applying the frequency control signal, the least three – for dithering. As a dither source either direct feedback or oscillator-based dither could be selected. Oscillator-based dither generator produces 1-bit dither for the least significant bit of the MASH modulator. To the second and third least significant bits logical '0' is applied.

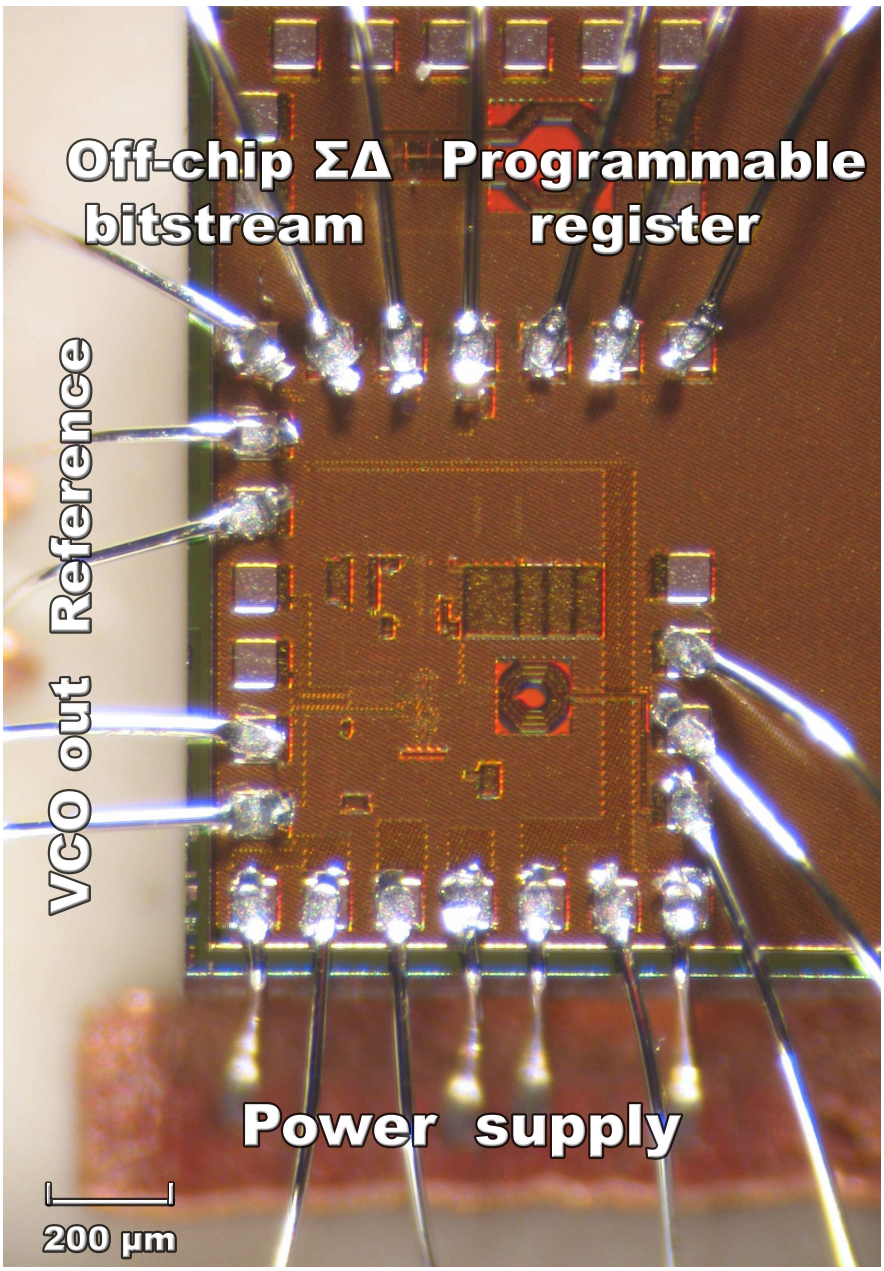


Figure 6.2: Bonded die photograph

6.1.1 Measurement Setup

Test Board

The fabricated chip is mounted on a printed circuit board (PCB) made of Rogers RO4003C material with the thickness of 508 μm and dielectric constant of $\epsilon_r = 3.38$. The layout of the printed circuit board is shown in Fig. 6.3.

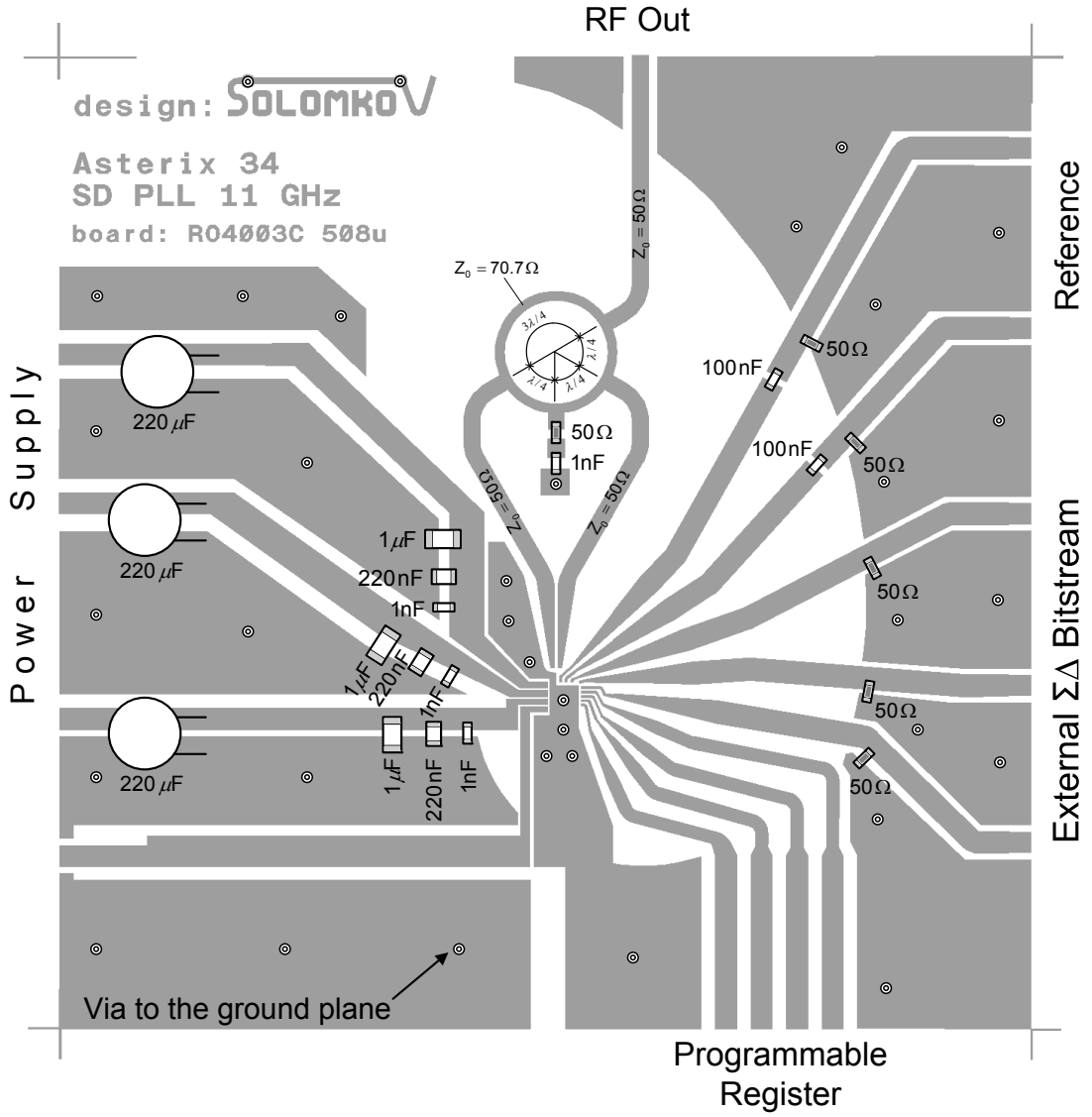


Figure 6.3: Test board layout

The 11 GHz differential output is combined on-board into the single-ended output by means of a rat-race balun [Pozar 90]. Due to the losses in PCB dielectric and mismatches, the power at single-ended output is around 2 dB higher than the power at each of the differential inputs (ideally, it should be 3 dB). Since all inputs

of the chip operating at reference frequency (reference source input, external sigma-delta modulator's bitstream input) are high ohmic, they are terminated by the 50 Ω resistors soldered on-board to minimize the reflections caused by the finite length of coaxial cables.

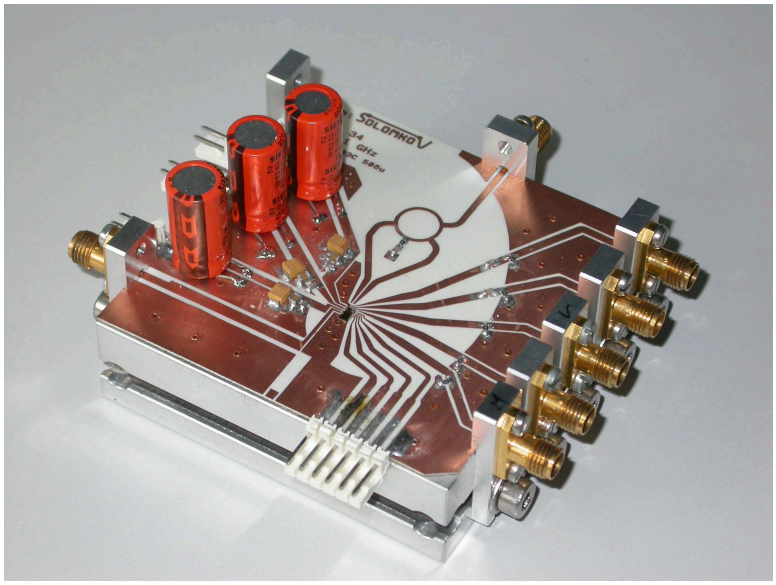


Figure 6.4: Test setup photograph

Special care is taken to minimize supply noise feedthrough. For this purpose each on-board supply line is bypassed to the ground plane by means of 4 capacitors soldered in parallel – 1 electrolytic lead capacitor with the nominal of 220 μF and three chip (SMD) capacitors with the nominals of 1 μF, 220 nF, and 1 nF. Such blocking scheme can suppress both low frequency noise components (220 μF lead capacitor) and high frequency noise components (3 chip capacitors) at the board supply lines. SMD capacitors are soldered as close to the chip as possible in order to make noise blocking more efficient.

Measurement Equipment and PLL Programming

For the measurements Agilent E4440A spectrum analyzer was used. Phase noise was measured by the Agilent E5052A signal source analyzer together with the Agilent E5053A microwave downconverter.

The PLL is controlled by means of on-chip programmable register. 4 terminals of the register are connected to the LPT port of a computer.

The application for programming the PLL is written in C++ programming language and its interface is shown in Fig. 6.5.

Some measurements (for example, fractional spurs power over the whole fractional division range) required automated procedure for controlling simultaneously de-

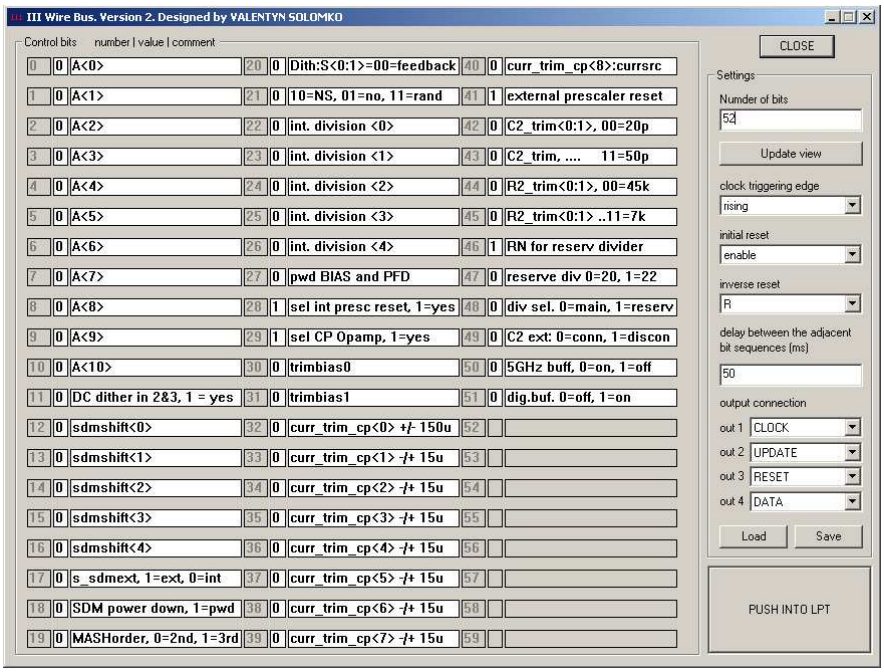


Figure 6.5: Interface of the application for programming the PLL

vice under test (PLL) and measurement equipment. In this case the procedure was realized in Matlab environment. From Matlab the implemented application for programming the device under test was used and measurement equipment was controlled via the GPIB interface.

FPGA-Based Sigma-Delta Modulator

An external FPGA-based sigma-delta modulator is used to verify the influence of internal sigma-delta modulator on the PLL spurious performance. The sigma-delta modulator generating the bitstream identical to the on-chip modulator is implemented in FPGA. When FPGA-based modulator is used for controlling the PLL, the on-chip modulator is kept disabled. The spurious performances measured with external and internal modulators are compared. The modulator is realized on a Hpe_mini test board with Altera Cyclone II FPGA. FPGA is clocked by the same reference quartz oscillator as used for synchronizing the PLL.

6.1.2 Performance Summary

The measured general performance of the 11 GHz PLL is summarized in Table 6.1. Measurements were done in fractional-N mode.

Phase noise plot for integer-N mode of operation is shown in Fig. 6.6. Measurements were performed for the VCO carrier frequency of 11.008 GHz. At this

Table 6.1: 11 GHz frequency synthesizer performance summary

Technology	0.13 μm CMOS
Supply voltage	1.5 V
Current consumption	50 mA
Reference frequency	64 MHz
Locking range	10.32 GHz – 11.2 GHz
Frequency resolution	31.25 kHz
Reference spurs	<–66 dBc @ f_{ref} <–58 dBc @ $2f_{ref}$
Fractional spurs	<–70 dBc within 70% of locking range
Phase noise	–83 dBc/Hz @ 10 kHz –80 dBc/Hz @ 1 MHz –115 dBc/Hz @ 10 MHz –140 dBc/Hz @ noise floor
Occupied area (including pads)	1000 μm × 800 μm

operating point the VCO gain reaches the value of 1.2 GHz/V. The loop bandwidth as high as 2 MHz ensures good phase noise suppression at low frequency offsets, keeping it below –90 dBc/Hz level.

The discrepancy of about 5 dB between the measured and simulated phase noise curves occurs within offset frequency range from 100 kHz to 2 MHz. In this range the VCO noise together with the charge pump noise dominate.

In Fig. 6.7 the phase noise of the PLL controlled by the MASH sigma-delta modulator is shown. The PLL operates with the average division ratio of 171.25. Such division ratio gives worst-case spurs, thus oscillator-based dithering is used to smooth the quantization noise of sigma-delta modulator and suppress fractional spurs at the output of the PLL.

The PLL bandwidth is set to the low value to avoid phase noise degradation caused by the quantization noise of MASH modulator. This, however, results in the increased noise in PLL bandwidth. The in-band noise of the PLL operating with sigma-delta modulator increases because of additional noise coming from the charge pump and probably because of sigma-delta quantization noise folding due to the nonlinearities in the PLL (this effect is not taken into account in the linear model). Charge pump current source matching circuitry linearizes slightly the charge pump – with disabled current source matching the in-band phase noise grows up by 2–3 dB.

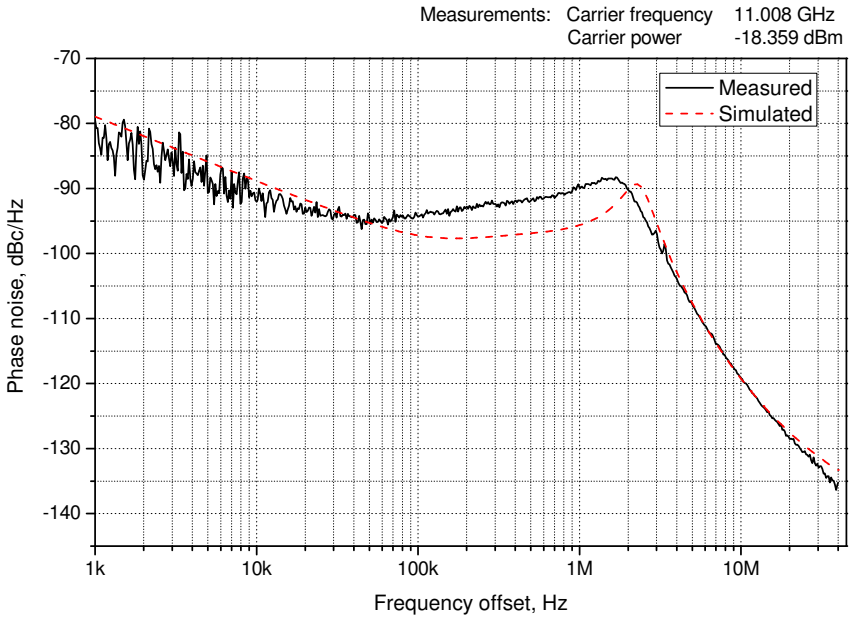


Figure 6.6: Measured phase noise of the PLL operating in integer-N mode

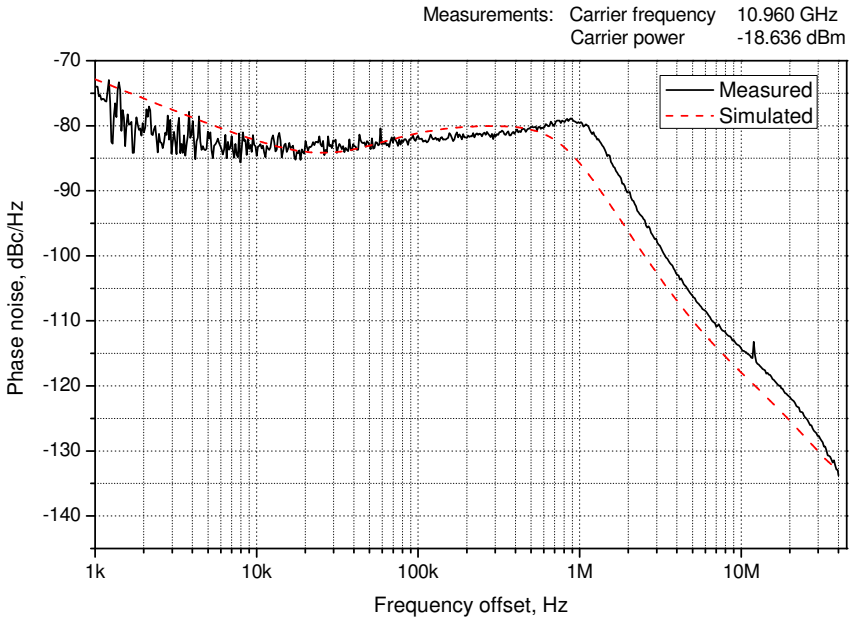


Figure 6.7: Measured phase noise of the PLL operating in fractional-N mode

6.1.3 Spurious Performance of the PLL Controlled by the Dual Edge Triggered MASH Modulator

The influence of dual edge triggered MASH modulator on the reference spurs performance is verified. The most straightforward way to compare the performance of PLL controlled by single- and dual edge triggered modulators would be to implement both structure on the same chip. However, due to the lack of silicon area single edge triggered MASH modulator was not integrated in the same die, thus the concept of dual edge triggering is verified indirectly.

The synthesizer features a possibility to use either internal (on-chip) modulator or external (off-chip) one implemented in Altera Cyclone II FPGA. Both FPGA-based and on-chip modulators generate identical digital sequence. When using external modulator, internal MASH is kept disabled. Digital bitstream from the off-chip modulator is constantly applied to the chip and disables internally when on-chip modulator is chosen (measurements showed that there is no visible change in PLL performance caused by the noise radiated from bitstream bondwires into the VCO tank).

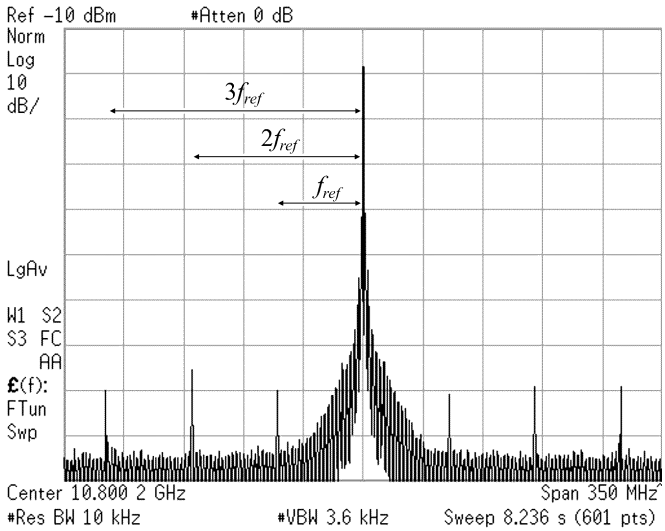
The measured reference spurs power for the case of on-chip and off-chip modulator is compared.

The PLL is synchronized by a 50 MHz crystal oscillator.

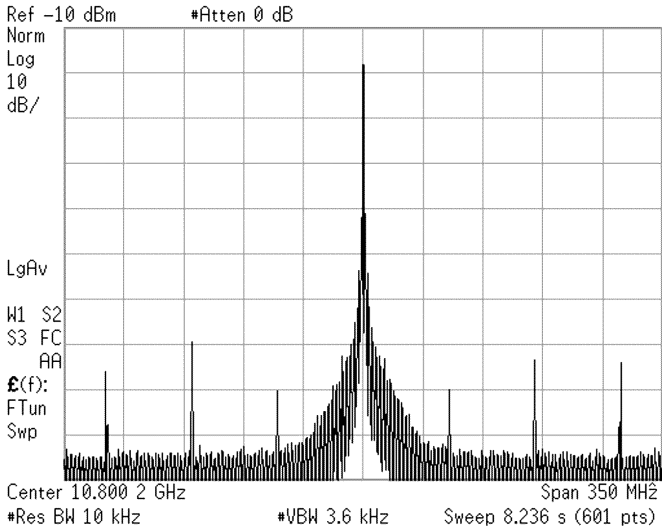
Fig. 6.8 demonstrates measured output spectrum of the synthesizer for fractional division ratio of 216.0078125. Switching noise couples mainly into the VCO inductor and loop filter capacitors (which altogether occupy around 11% of PLL area). With enabled on-chip modulator second and third reference spurs increase by 5 dB and 4 dB respectively, while the power of first spur remains the same. This implies that supply noise crosstalk is a dominating factor for spurs at $2f_{ref}$ and $3f_{ref}$, while the first one is not caused by the supply noise induced by sigma-delta modulator. Even though the amplitude of a third harmonic in switching noise spectrum of MASH 1-1-1 modulator is low (see Fig. 4.33), the coupling for higher frequencies is stronger because of the capacitive path between VCO inductor and substrate. This explains such significant change in third spur level.

The diagrams in Fig. 6.9 show reference spurs behavior versus generated VCO carrier frequency. With enabled on-chip modulator first reference spur is below the second one over the whole locking range. Because of the switching current distribution, the power of the first spur does not increase with enabling the internal modulator. At carrier frequency of 10.9 GHz it reaches the lowest level due to the best charge pump current source matching in the vicinity of 1.1 V. At this point the first spur with enabled external modulator is even higher. This can be explained by switching noise coupling coming from the 3 pad buffers and ESD structures for the external modulator's sequence.

Fig. 6.9(b) proves that the dominating source of the second reference spur is a digital noise from the internal sigma-delta modulator. With disabled on-chip



(a)



(b)

Figure 6.8: Measured output spectrum of the synthesizer: (a) – with off-chip modulator, (b) – with on-chip modulator

modulator second spur falls down by 5 dB.

Switching noise content is almost independent on MASH control signal (namely, fractional part of the division ratio). However, spurious power depends on the gain of locked VCO: curves in Fig. 6.9(a) and Fig. 6.9(b) roll off at the edges of the locking range. Current mismatches give 6 dB lower spur at f_{ref} for twice reduced VCO gain. The harmonic at $2f_{ref}$ coupled into the loop filter also has less impact if the VCO gain is lower.

Measurements showed that switching action of the dual edge triggered modula-

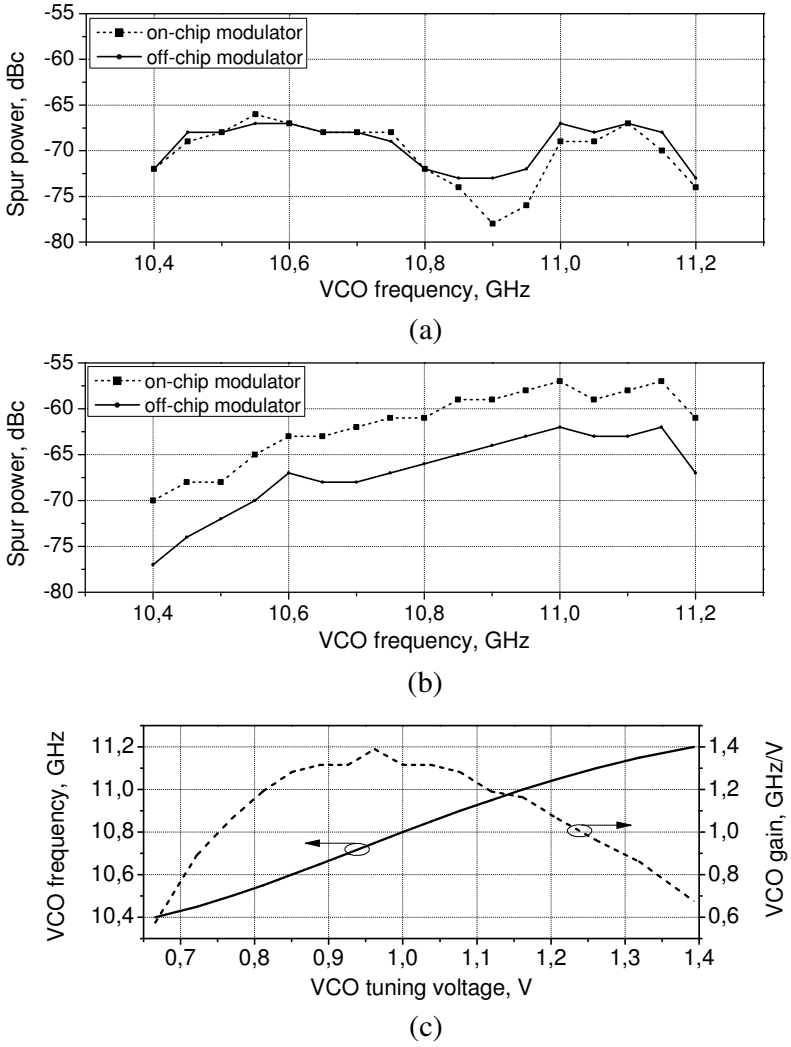


Figure 6.9: Measured reference spurs power versus VCO frequency change. Spurs at (a) – f_{ref} offset, (b) – $2f_{ref}$ offset from the carrier; (c) – VCO tuning curve and gain

tor does not degrade first reference spur of a synthesizer. Instead, it pushes the switching noise energy to the even multiplies of reference frequency.

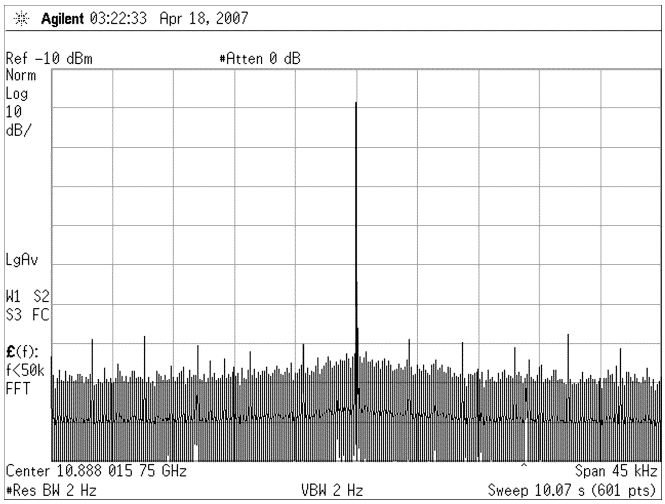
6.1.4 PLL Performance Controlled by the MASH Modulator Employing Oscillator-Based and Direct Feedback Dithering

As it was proved by the simulations, the minimum resolution required for the modulator to use direct feedback dithering is 7 bits. An FPGA-based modulator was developed to verity the simulation results. The measurements confirmed the simulations: PLL controlled by the modulator with resolution less than 7 bits generated unstable carrier with a big amount of severe fractional spurs; MASH modulators with the resolution of 7 bits and higher dithered by their own output signal demonstrated stable operation without powerful harmonics (in all the cases dither was applied to the three least significant bits of the first accumulator).

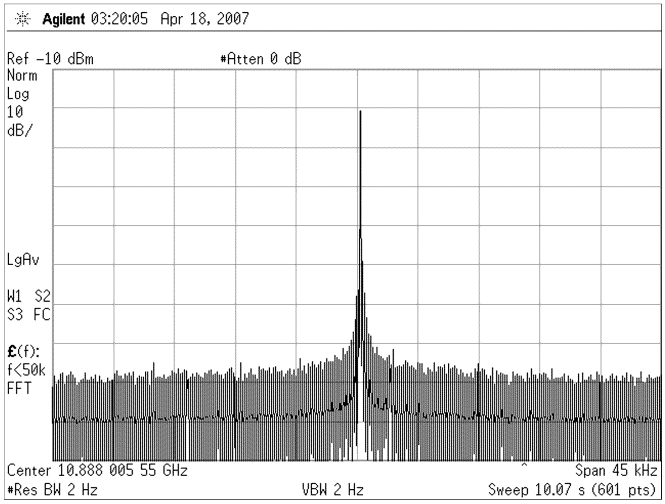
The comparison of PLL spurious performance controlled by the on-chip MASH modulator with direct feedback dithering and oscillator-based dithering was done. Fig. 6.10 demonstrates measured output spectrum of the PLL for both cases. The span of the observed spectrum is 45 kHz. As it can be seen from Fig. 6.10(a), direct feedback dither does not suppress the tones totally and some low power spurs at low frequency offsets are still visible. Oscillator-based dither generator smoothes the phase noise of the PLL, that no harmonics are any more visible in the power spectrum measured with the same resolution bandwidth, see Fig. 6.10(b). In the case of oscillator-based dither generator spurs are distributed at the expense of slightly increased phase noise at very low frequency offsets (can be seen in the measured spectrum).

For performing the measurements the bandwidth of the PLL was set to the highest value to suppress the in-band charge pump noise, otherwise fractional spurs could not be visible even with the lowest resolution bandwidth available in spectrum analyzer.

The fractional spurs demonstrated so far were caused by the tonal behavior of sigma-delta modulator. The PLL output spectrum contain another fractional spurs produced by the nonlinearities in the analog part. They are observed within the span of 20 MHz. Over this span spurious tones up to 10 MHz apart from the carrier could be detected. In order to distinguish low power spurious in the phase noise of the output signal, a resolution bandwidth of the spectrum analyzer was set to the low value. This made a measurement procedure very time consuming – it took more than 26 minutes to proceed one 20 MHz sweep. The PLL spurious performance for all possible fractional division ratios in the range from 170 to 171 was estimated. Each high frequency carrier generated within this range contained maximum two dominant fractional spurious tones. Fig. 6.11 shows an example of the measured PLL output spectrum. Two fractional spurs with the power of –74 dBc and –82 dBc at 4 MHz and 8 MHz apart from the carrier are clearly seen at the measured spectrum. The diagram showing the dependence of spurious power and offset on the fractional part of the division ratio (which equals the modulator's control word) is plotted in Fig. 6.12. For some division ratios one



(a)



(b)

Figure 6.10: Measured power spectrum of the PLL output signal observed over a 45 kHz span: (a) – operating with direct feedback dithering, (b) – dither is generated by means of ring oscillator

or both spurs were either hidden in the phase noise or were out of the observed span, making the breaks in plotted curves.

The non-symmetrical spurious distribution just tells, that they have nothing to do with the intrinsic tones in digital sigma-delta modulator, but caused by the influence of nonlinearities which alter with the change of operating point (namely, division ratio). Within the other range of integer division ratios fractional spurs power/offset distribution will be different. This is explained by the fact that operating points of all the analog blocks which introduce nonlinearities (charge pump, VCO) change. Spurs distribution does not depend on the dithering topology.

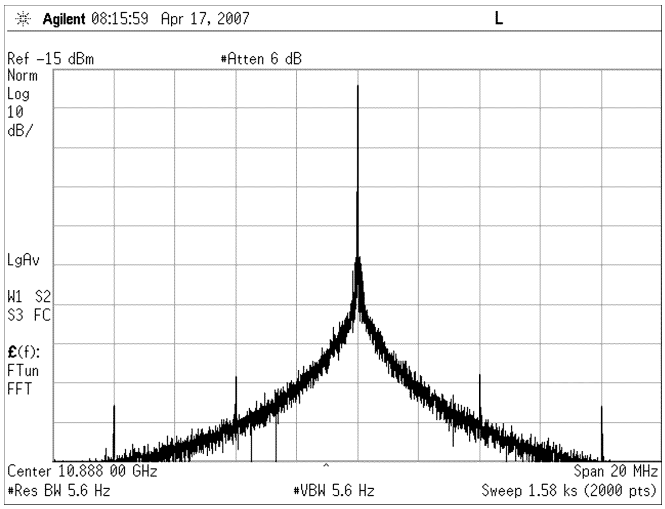


Figure 6.11: Power spectrum of the PLL output signal observed over a 20 MHz span. Operating conditions: reference frequency f_{ref} = 64 MHz; division ratio N = 170.125; oscillator-based dithering is used

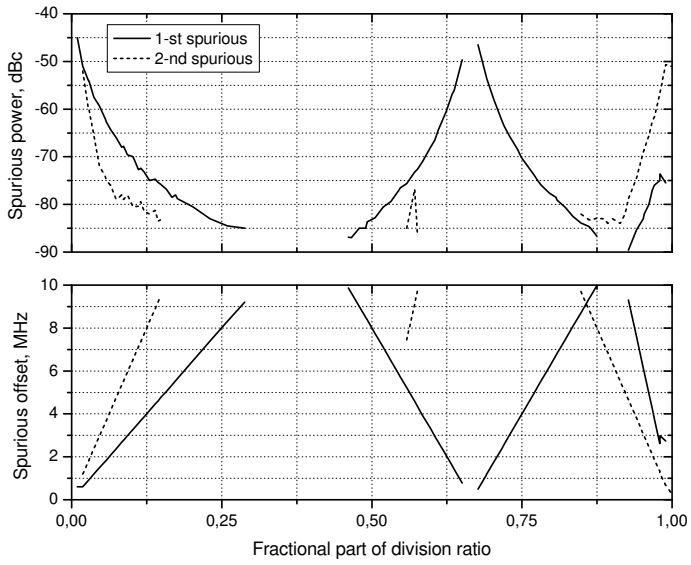


Figure 6.12: Spurious distribution over the fractional part of division ratio

According to the diagram in Fig. 6.12 fractional spurs power does not exceed –70 dBc within 70% of the division ratio range.

6.2 Monolithically Integrated 11 GHz Sigma-Delta PLL Employing MASH Modulator with DC Dithering

The 11 GHz CMOS fractional-N PLL employing MASH modulator with DC dithering was fabricated in 0.13 μm CMOS technology. The goal of the implemented PLL is to verify the spurious performance of the fractional-N PLL controlled by the MASH 1-1-1 modulator with DC dithering.

This implementation is pretty much similar to the one described in Section 6.1. The main differences are in the divider construction and sigma-delta modulator. The charge pump incorporates some minor changes as well. The overall performance of the implemented device is similar to the PLL demonstrated in previous section.

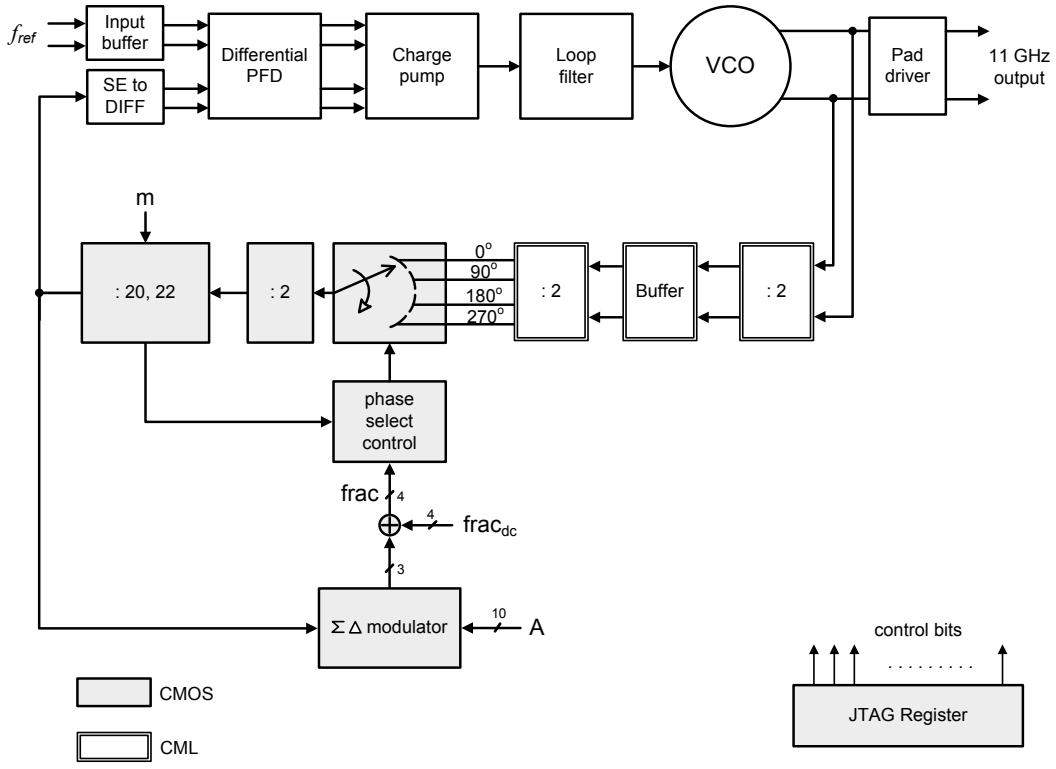


Figure 6.13: Block diagram of the PLL

Fig. 6.13 illustrates the block diagram of the implemented PLL. Sigma-delta modulator is realized as a MASH 1-1-1 modulator with 10-bit input word. Second and third stages of MASH modulator incorporate additional dithering bits resulting in 12- and 14-bit resolution respectively. Referring to Fig. 4.36: $k = 10$, $m_1 = 2$, $m_2 = 2$. The simulation results for the realized modulator are presented in Section 4.7.3.

The die photograph is shown in Fig. 6.14.

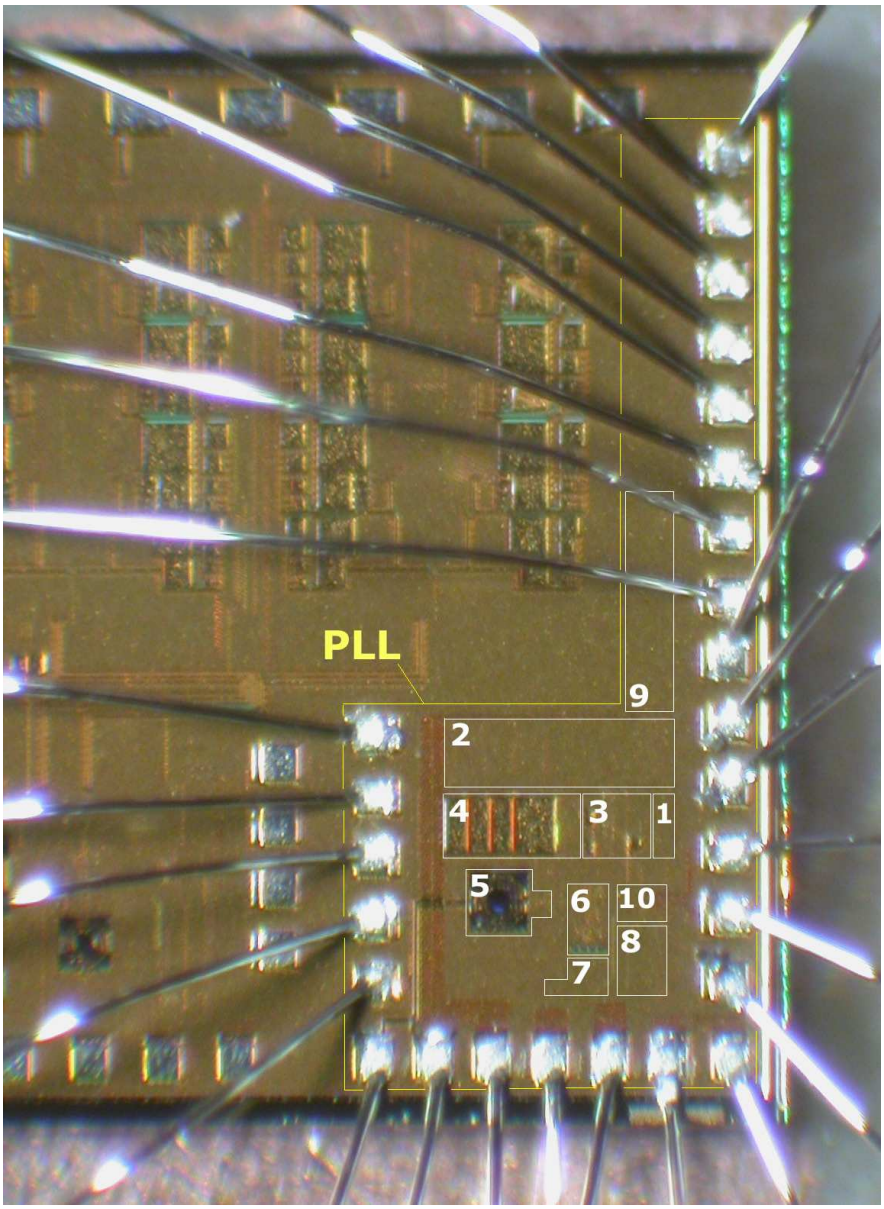


Figure 6.14: Chip layout. Blocks numeration: 1 – input buffer, 2 – bandgap reference, 3 – CP and PFD, 4 – loop filter, 5 – VCO, 6 – CML divider, 7 – prescaler, 8 – sigma-delta modulator, 9 – programmable register, 10 – 11 GHz pad driver

The reference frequency used for PLL measurements is 64 MHz. The bandwidth is chosen to be more than 1 MHz which results on one hand in phase noise degradation at frequency offsets from 5 MHz to 40 MHz due to the quantization noise of the third order sigma-delta modulator, but on the other hand clearly visible fractional spurs within the PLL bandwidth which are aimed to be compared for the case of dithered and undithered modulator.

Table 6.2: 11 GHz frequency synthesizer performance summary

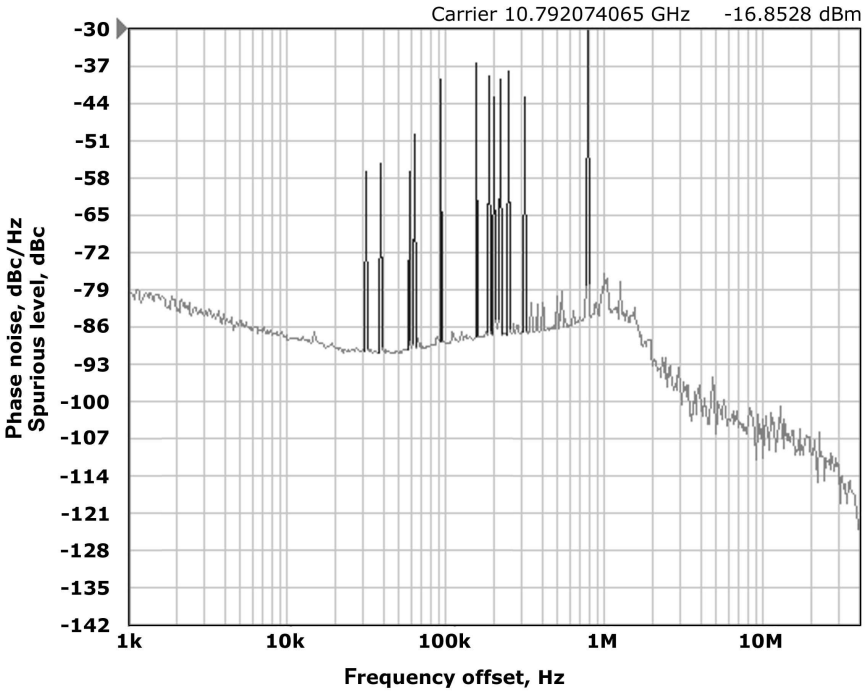
Technology	0.13 μm CMOS	
Supply voltage	1.5 V	
Current consumption	63 mA	
Occupied area	800×800 μm	
Reference frequency	64 MHz	
Output frequency range	PLL capture range	10.24 - 12.55 GHz (18%)
	VCO tuning range	10.6 - 11.6 GHz (9.1%)
Frequency resolution	125 kHz	
Phase noise	In-band phase noise	<–80 dBc/Hz
	Noise floor	–140 dBc/Hz
Reference spurs	–52 dBc	
Fractional spurs	–44 dBc	
Maximum lock time	8 μs	

The measured phase noise/spurious diagram of the generated signal for the case of undithered modulator is demonstrated in Fig. 6.15(a). The fractional control word is set to 0.3134765625 corresponding to the following binary representation: $A_{k-1\ldots0}[n] = 0101000001_2$. The least significant bit of the input word switched to '1' ensures the best-case spurious performance of undithered modulator. Synchronized with a reference frequency of $f_{ref} = 64$ MHz the spurious will appear at frequency offsets of $n \cdot (f_{ref}/(2 \cdot 2^k)) = n \cdot 31.25$ kHz apart from the carrier which is confirmed by the measurements. The power of some fractional spurs in the obtained diagram exceeds –30 dBc level. Most of the spurs are well above –40 dBc.

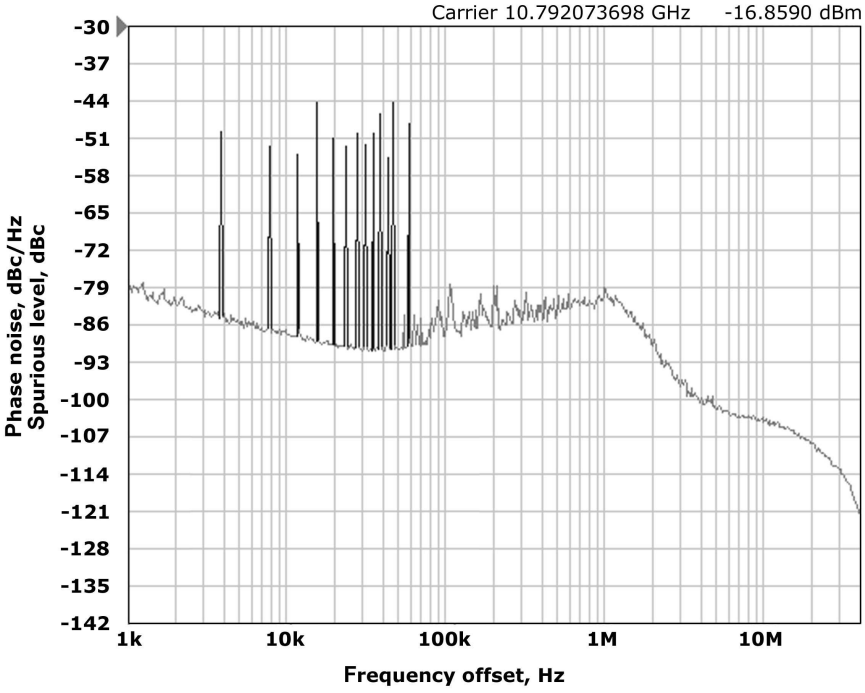
After adding dithering signal to the subsequent accumulators, spurs move to the lower frequency offsets and their power decreases, yielding the spurious at frequency offsets $n \cdot (f_{ref}/2^{k+m_1+m_2})$, where $k+m_1+m_2 = 14$ is the number of bits in the third stage of the MASH modulator. The measured phase noise/spurious plot with dithered modulator is presented in Fig. 6.15(b). The fractional spurs are observed at frequency offsets of $n \cdot 3.9$ kHz and their power does not exceed –44 dBc level. Measurements confirm the simulation results.

Some of the observed spurious tones (at frequencies 38.8 kHz, 58.5 kHz and 200 kHz) common for both phase noise diagrams are caused by the external factors: the second is generated by the reference crystal oscillator, and 200 kHz spur is probably introduced by the power supply cables, since 200 kHz is a common switching power supply frequency.

The overall synthesizer performance summary is presented in Table 6.2. The sigma-delta modulator changes the division ratio not with a unity step, but with a step of 2, which results in the frequency resolution of 125 kHz.



(a)



(b)

Figure 6.15: Measured phase noise/spurious diagram with (a) – disabled DC dithering in second and third stages, (b) – DC dither applied to the second and third stages

Chapter 7

Conclusion

The current trend shows, that fully integrated sigma-delta frequency synthesizers realized in submicron CMOS technologies will soon become dominant in portable, low-cost wireless transceivers. In the current work mixed-signal interaction aspects, which appear to be a bottleneck in integrated sigma-delta frequency synthesizer design, and optimized solutions for digital sigma-delta modulators are investigated. Several different implementations of digital sigma-delta modulators were described. The research focuses mainly on improvement of MASH 1-1-1 modulator as one of the most efficient and widely used architectures at present time. The described implementations offer reduction in area, advantageous switching noise distribution, and good tonal performance. The measurements of the fully integrated 11 GHz PLL fabricated in 0.13 μm CMOS technology prove theoretical findings and simulation results.

The main achievements of the work are summarized below.

1. A dual edge triggered MASH modulator implemented in CMOS logic is proposed. The implementation distributes the switching noise power in such a manner that the first reference spur of a synthesizer is not degraded; instead, the glitch energy is shifted to the second multiple of reference frequency. Modulator's area is reduced by 15–20%. Possible application of the sigma-delta PLL controlled by the dual edge triggered modulator is a frequency synthesizer in an integrated transceivers working with ISM band standards with RF bandwidth below 200 MHz.

2. MASH 1-1-1 (three stages of first order each) sigma-delta modulator with DC dithering used for frequency synthesis applications is proposed [Solomko 06]. At the expense of minimum additional hardware such dithering topology allows to shift tones to the low frequencies and decrease their power.

3. An oscillator-based dither generator is proposed for the use in MASH 1-1-1 modulator. The generator consumes less current and area, produces much less supply switching noise than a conventional pseudo-random dither

generator, while keeping modulator's output free of tones. An empirical study of oscillator-based dither generator is presented.

4. MASH 1-1-1 modulator with direct feedback dithering is investigated. With a little penalty in tonal performance, such dithering topology requires no additional hardware to be implemented.

Possible applications for described modulators are low cost, fully integrated sigma-delta frequency synthesizers fabricated in submicron CMOS technologies.

Appendix A

Frequency Divider Implementation

A.1 Circuit Implementation of DX_1 Block

DX_1 is a part of the frequency divider shown in Fig. 5.25. It operates at frequency of 1.4 GHz. In Fig. A.1 the internal structure of DX_1 is shown.

A heart of DX_1 is a 5-bit resettable counter CR. Its circuit diagram is demonstrated in Fig. A.3. CR is a pipelined and optimized version of a synchronous ripple-carry counter presented in [Stan 98]. The propagation path is partitioned with a flip-flop placed between the third and fourth stages of a counter allowing the device to operate at frequency of 1.4 GHz. Simulated maximum critical propagation delay is 7 times shorter than the period of triggering signal (which equals 1/(1.4 GHz)). Such significant margin ensures the operability of the counter even with the presence of simulation inaccuracies and additional increase of propagation delay caused by layout parasitics (which were not taken into account in the simulation). In order to provide bit-parallel output deskewing flip-flips are added after the first three stages of the counter.

In the circuit both static (DFF_{SET}) and dynamic (DFF_D) flip-flops are used. When no reset function is required dynamic flip-flops are preferable because of a smaller occupied area and 4 times lower average and peak supply current than in static DFFs. Transistor implementation of DFF_D is shown in Fig. A.7.

All blocks of DX_1 are clocked by the input signal Fin. Counter CR generates digital ramp signal appearing at the bus b<0:4>. At each triggering step it is compared with the control word (*int*) which defines the division ratio. When the value accumulated by the counter reaches half of the desired division ratio $COMP_1$ resets the RS-flip-flop RSFF and it generates the falling edge of the output signal Fout. When the value at b<0:4> becomes equal to the desired division ratio, $COMP_2$ sets the output of RSFF to '1' (generating the rising edge at the port Fout) and resets the counter.

Since the counter is pipelined and a register is placed at its output (see Fig. A.3) it required two dummy clock cycles before outputting the ramp signal. Moreover, one cycle of Fin is skipped during the reset of the counter and another one unity delay is caused by the D-flip-flop at the output of $COMP_2$ (see circuit diagram). In order to make the division ratio equal to the control signal *int*, the value of 4 is subtracted from the *int* before applying it to the comparators $COMP_1$ and $COMP_2$. Block AD5 performs the subtraction. For this reason the values 1, 2, 3, and 4 for the control signal *int* are prohibited and they must fall in the range $int \in [5; 31]$.

The other blocks of DX_1 are responsible for generating triggering pulses for phase selector. As a source of pulses Fin signal is used. $frac$ value defines the number of pulses. At each triggering step block COMPT compares the output value of the counter b with the desired value $frac$ and enables the gated clock cell CLKG latched by Fin until $frac \leq b$. During this time CLKG outputs the signal applied to its clock input. When the counter value exceeds the control word $frac$ COMPT generates disabling signal for gated clock cell and no more pulses appear at the output *pulse* until the next rising edge of divided signal Fout. Four dynamic flip-flops connected in series are aimed at compensating the 4-cycle delay introduced by the comparator $COMP_2$ and the counter.

Since pulse count is defined between two rising edges of the divided signal for guaranteeing correct instantaneous division ratio phase-frequency detector must be rising-edge triggered.

The value $frac$ falls in the range: $frac \in [1; int - 4]$. The value of $frac = 0$ is prohibited, since in such case the maximum number of pulses will be generated.

Fig. A.2 illustrates timing diagram of DX_1 block for control words $int = 10$, $frac = 3$.

A.2 Prescaler Start-Up Circuit

Start-up circuit serves for generating triggering signal for prescaler when it drives into the latched state and no AC signal appears at its output. The start-up circuit is presented in Fig. A.10 and operates as follows. Reference signal is applied to the frequency divider formed by the three DFF_{SET} flip-flops with a feedback loop. Each flip-flop has an inverted reset terminal. When logical '1' is applied to the RN terminals, meaning that no reset takes place, than the divider generates digital signal with a 6 times lower rate than the reference one. This signal is applied to the output terminal of the block and serves as a start-up for the prescaler.

This, however, happens only if divided signal is not active, meaning that prescaler is in latched state, and either static '0' or static '1' appears at terminal div. If the divider's signal changes its logical level periodically pulse generator made of four inverters I_1 – I_4 and NXOR gate NX_1 produces short negative pulses (with

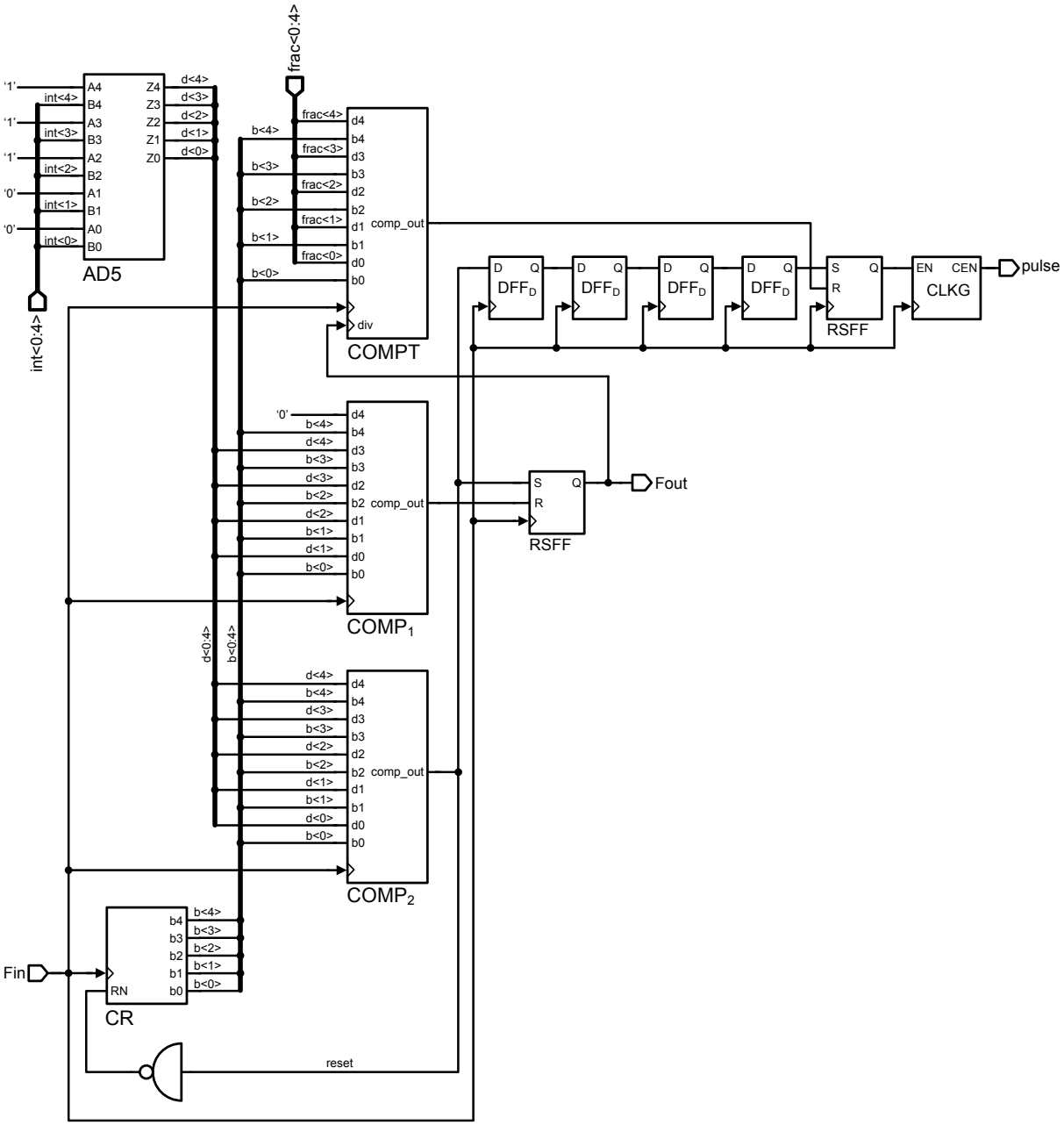


Figure A.1: DX_1 block diagram

the width defined by the propagation delay of the seriesly connected inverters) which reset the flip-flops not allowing any start-up signal to reach the output. Transistors M_{n1} and M_{n2} enlarge the pulse width that it could be enough to reset the flip-flops.

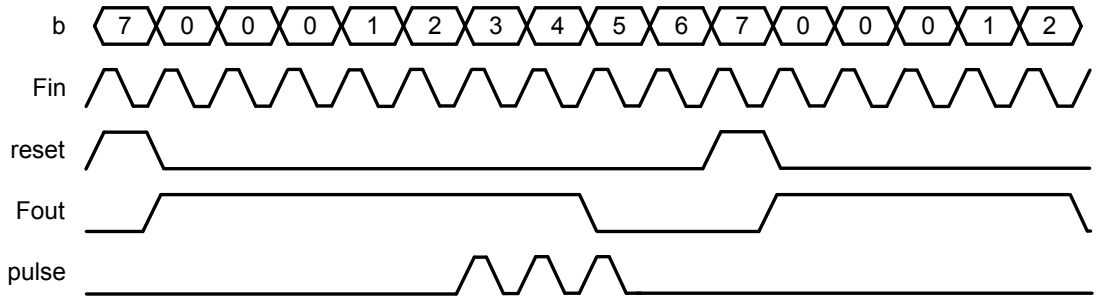


Figure A.2: Timing diagram of DX_1 for int = 10, frac = 3

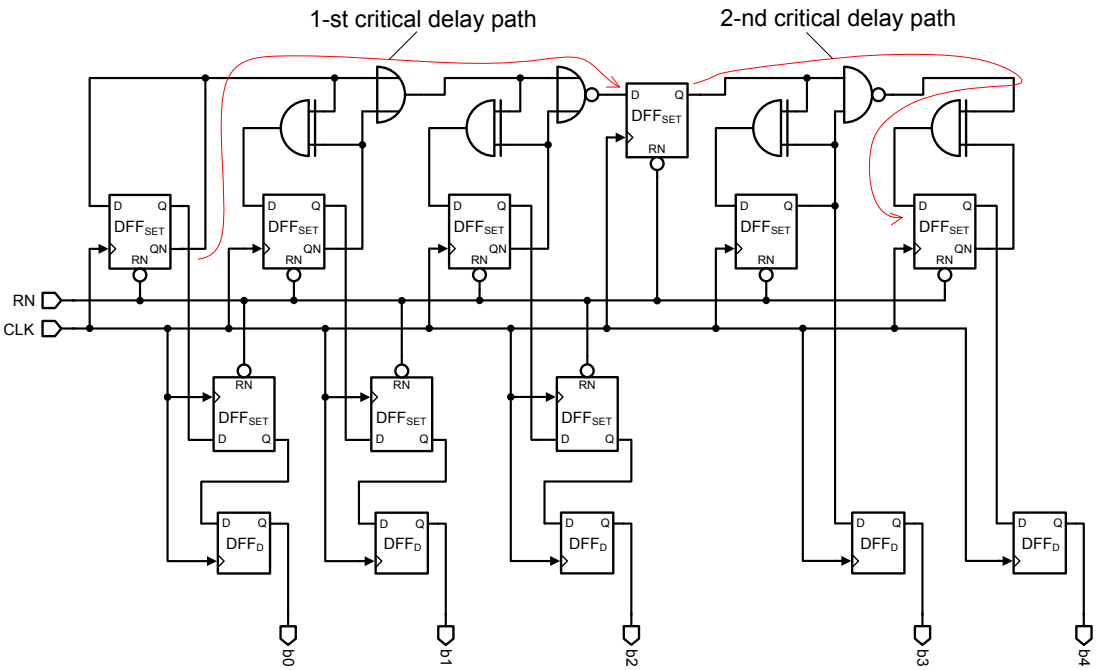


Figure A.3: 5-bit counter (CR) circuit diagram

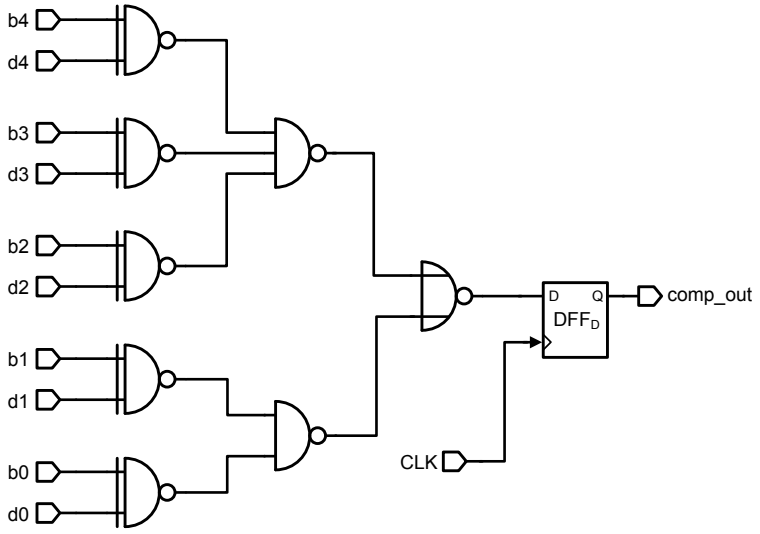


Figure A.4: $COMP_1/COMP_2$ circuit diagram

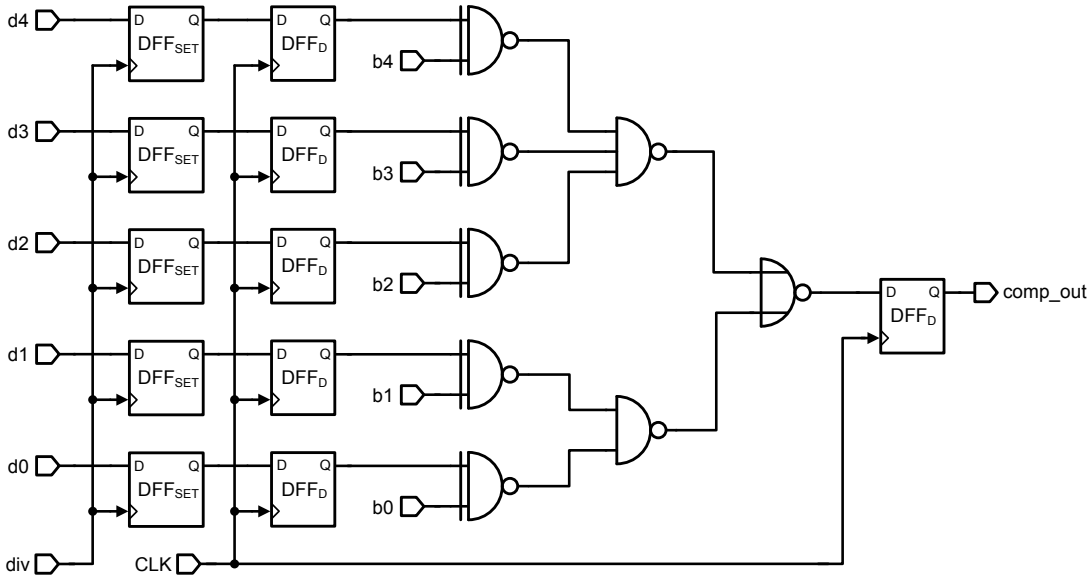


Figure A.5: COMPT circuit diagram

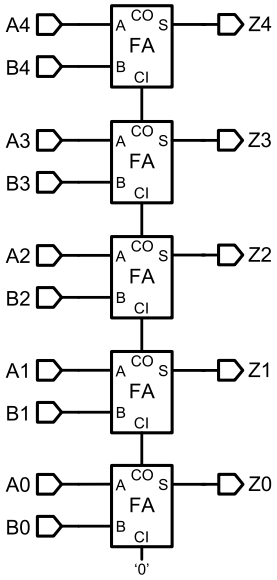


Figure A.6: AD5 circuit diagram

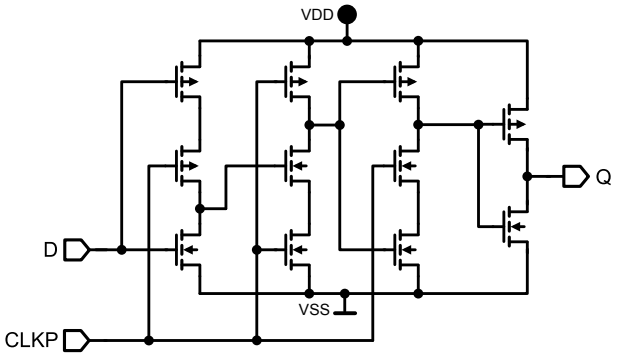


Figure A.7: DFF_D circuit diagram

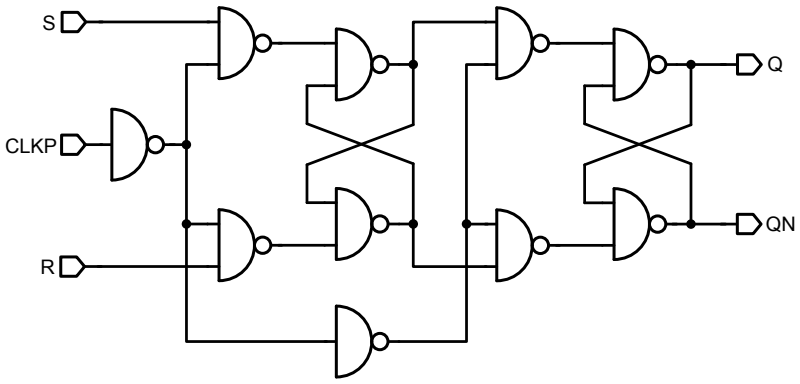


Figure A.8: Edge-triggered RS-flip-flop (RSFF) circuit diagram

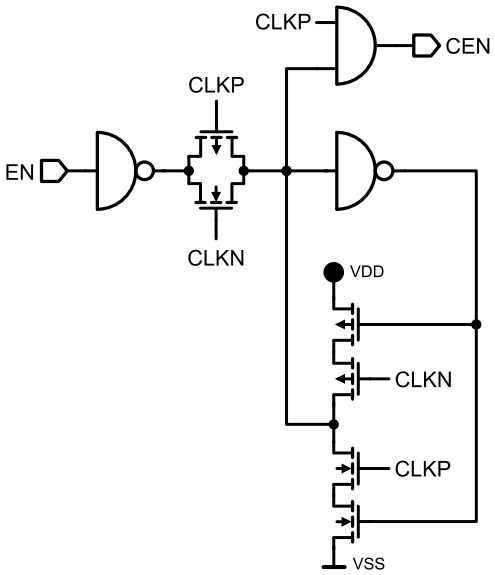


Figure A.9: Latched gated clock cell CLKG circuit diagram

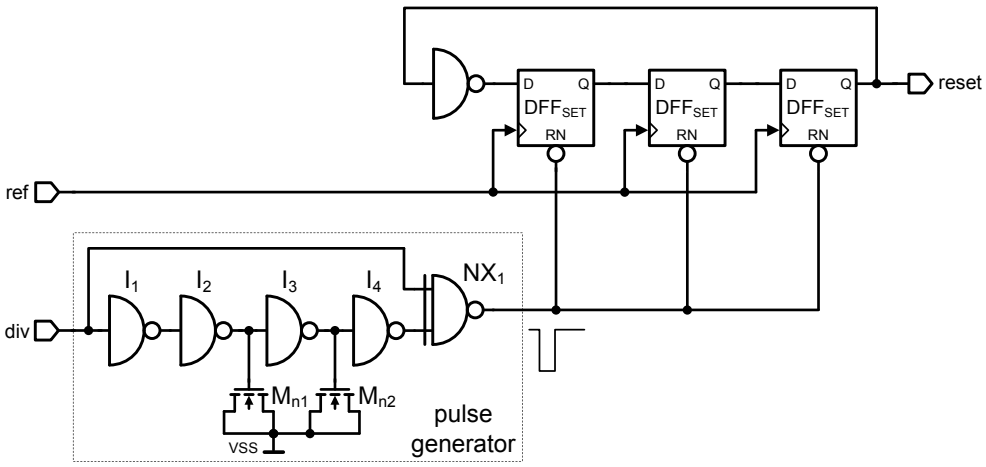


Figure A.10: Prescaler start-up circuit implementation

Bibliography

[Abidi 04] Asad A. Abidi, "RF CMOS comes of age", *IEEE journal of solid-state circuits*, vol. 39, no. 4, pp. 549–561, April 2004.

[Aparicio 02] Roberto Aparicio and Ali Hajimiri, "Capacity limits and matching properties of integrated capacitors", *IEEE journal of solid-state circuits*, vol. 37, no. 3, pp. 384393, March 2002.

[Backenius 07] Erik Backenius, *Reduction of substrate noise in mixed-signal circuits*, PhD thesis, Department of Electrical Engineering, Linköping University, SE-581 83 Linköping, Sweden, 2007.

[Badaroglu 05] Mustafa Badaroglu, Piet Wambacq, Geert Van der Plas, Stéphane Donnay, Georges G. E. Gielen, and Hugo J. De Man, "Digital ground bounce reduction by supply current shaping and clock frequency modulation", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 24, no. 1, pp. 65–76, January 2005.

[Borkowski 05] Maciej Jan Borkowski and Juha Kostamovaara, "Spurious tone free digital delta-sigma modulator design for DC inputs", *in IEEE International Symposium on Circuits and Systems*, pp. 5601–5604, May 2005.

[Bornoosh 05] Babak Bornoosh et al., "Reduced complexity 1-bit high-order digital delta-sigma modulator for low-voltage fractional-N frequency synthesis applications", *IEE Proceedings on Circuits, Devices, and Systems*, vol. 152, no. 5, pp. 471–477, October 2005.

[Brandtner 02] Thomas Brandtner and Robert Weigel, "Hierarchical simulation of substrate coupling in mixed-signal ICs considering the power supply network", *in Design, Automation and Test in Europe Conference and Exhibition*, pp. 1028–1032, Paris, France, 2002.

[Brennan 04] Paul V. Brennan, Paul Radmore, and Dai Jiang, "Intermodulation-borne fractional-N frequency synthesiser spurious components", *IEE Proceedings on Circuits, Devices and Systems*, vol. 151, no. 6, pp. 536–542, December 2004.

[Chen 00] Hwan-Mei Chen, Ming-Hwei Wu, B.C. Liau, Laurence Chang, and Ching-Fu Wu, "The study of substrate noise and noise-rejection-efficiency of guard-ring in monolithic integrated circuits", *in IEEE International Symposium on Electromagnetic Compatibility*, pp. 123–128, 21-25 August 2000.

[Chen 06] Wei-Zen Chen and Dai-Yuan Yu, "A dual-band four-mode $\Sigma\Delta$ frequency synthesizer", *IEEE Radio Frequency Integrated Circuits Symposium*, 11-13 June 2006.

[Chou 91] Wu Chou and Robert M. Gray, "Dithering and its effects on sigma-delta and multistage sigma-delta modulation", *IEEE Transactions on Information Theory*, vol. 37, no. 3, pp. 500–513, May 1991.

[Craninckx 96] Jan Craninckx and Michel S. J. Steyaert, "A 1.75-GHz/3-V dual-modulus divide-by-128/129 prescaler in 0.7-μm CMOS", *IEEE journal of solid-state circuits*, vol. 31, no. 7, pp. 890–897, July 1996.

[Craninckx 98] Jan Craninckx and Michel S. J. Steyaert, "A fully integrated CMOS DCS-1800 frequency synthesizer", *IEEE journal of solid-state circuits*, vol. 33, no. 12, pp. 2054–2065, December 1998.

[Cutler 60] Cassius C. Cutler, *Transmission Systems Employing Quantization*, U.S. Patent No. 2,927,962, March 8, 1960, (filled 1954).

[Dalt 02] Nicola Da Dalt and Christoph Sandner, "A subpsec jitter PLL for clock generation in 0.12 μm digital CMOS", *in 28th European Solid-State Circuits Conference*, pp. 415–418, 24-26 September 2002.

[Debski 07] Wojciech Debski, *Multi-band Adaptive WLAN Receivers in 0.13 μm CMOS*, PhD thesis, Chair of Circuit Design, Brandenburg University of Technology Cottbus, Erich-Weinert-Str. 1, D-03046 Cottbus, Germany, June 2007.

[Ding 07] Yanping Ding and Kenneth K. O, "A 21-GHz 8-modulus prescaler and a 20-GHz phase-locked loop fabricated in 130-nm CMOS", *IEEE journal of solid-state circuits*, vol. 42, no. 6, pp. 1240–1249, June 2007.

[Ebert 05] Jean-Pierre Ebert, Eckhard Grass, Ralf Irmer, Rolf Kraemer, Gerhard Fettweis, Karl Strom, Günther Tränkle, Walter Wirnitzer, Reimund Witmann, Hans-Jürgen Reumerman, Egon Schulz, Martin Weckerle, Peter Egner, and Ulrich Barth, "Paving the way for gigabit networking", *IEEE Communications Magazine*, vol. 43, no. 4, pp. 27–30, April 2005.

[Eynde 01] Frank Op't Eynde et al., "A fully-integrated single-chip SOC for Bluetooth", *in IEEE Solid-State Circuits Conference*, pp. 196–197, San Francisco, CA, USA, 2001.

[Fukuda 01] Yasuhiro Fukuda, Shuji Ito, and Masahiro Ito, "SOI-CMOS device technology", *OKI technical review*, vol. 68, no. 4, pp. 54–57, March 2001.

[Gal 95] Laszlo Gal, "On-chip cross talk – the new signal integrity challenge", *in Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 251–254, 1-4 May 1995.

[Gillette 69] Garry C. Gillette, "The digiphase synthesizer", *in 23rd Annual Frequency Control Symposium*, pp. 25–29, April 1969.

[Greenhouse 74] Harold M. Greenhouse, "Design of planar rectangular microelectronic inductors", *IEEE transactions on parts, hybrids, and packaging*, vol. PHP-10, no. 2, pp. 101–109, June 1974.

[Hasting 01] Alan Hasting, *The Art of Analog Layout*, Prentice Hall, New York, first edition, 2001.

[Hegazi 03] Emad Hegazi and Asad A. Abidi, "A 17-mW transmitter and frequency synthesizer for 900-MHz GSM fully integrated in 0.35-μm CMOS", *IEEE journal of solid-state circuits*, vol. 38, no. 5, pp. 782–792, May 2003.

[Heller 84] Lawrence G. Heller and William R. Griffin, "Cascode voltage switch logic: a differential CMOS logic family", *IEEE Solid-State Circuits Conference, Digest of Technical Papers*, vol. XXVII, pp. 16–17, February 1984.

[Hernandez 96] Luis Hernandez, "Frequency synthesis based on bandpass sigma-delta modulation", *IEE Electronics Letters*, vol. 32, no. 18, pp. 1642–1643, August 1996.

[Heydari 04] Payam Heydari, "Analysis of the PLL jitter due to power/ground and substrate noise", *IEEE Transactions on Circuits And SystemsI*, vol. 51, no. 12, pp. 2404–2416, December 2004.

[Hossain 94] Razak Hossain, Leszek D. Wronski, and Alexander Albicki, "Low power design using double edge triggered flip-flops", *IEEE Transactions on VLSI Systems*, vol. 2, no. 2, pp. 261–265, June 1994.

[Jenkins 06] Keith A. Jenkins, Woogeun Rhee, John Liobe, and Herschel Ainspan, "Experimental analysis of the effect of substrate noise on PLL performance", *in Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 54–57, January 2006.

[Jiang 04] Yingtao Jiang, Abdulkarim Al-Sheraidah, Yuke Wang, Edwin Sha, and Jin-Gyun Chung, "A novel multiplexer-based low-power full adder", *IEEE Transactions on Circuits and Systems II*, vol. 51, no. 7, pp. 345–348, July 2004.

[Johns 97] David Johns and Ken Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, New York, first edition, 1997.

[Kehrer 03] Daniel Kehrer, *40 Gb/s High Speed Circuits in Standard CMOS Technology*, PhD thesis, Technische Universität Wien, Hacklweg, March 2003.

[Kingsford-Sm 75] Charles A. Kingsford-Smith, *Device for synthesizing frequencies which are rational multiplies of a fundamental frequency*, U.S. Patent No. 3,928,813, December 23, 1975, (filled 1974).

[Larsson 97] Patrik Larsson, "Parasitic resistance in an MOS transistor used as on-chip decoupling capacitance", *IEEE journal of solid-state circuits*, vol. 32, no. 4, pp. 574–576, April 1997.

[Larsson 98] Patrik Larsson, "Resonance and damping in CMOS circuits with on-chip decoupling capacitance", *IEEE Transactions on Circuits And SystemsI*, vol. 45, no. 8, pp. 849–858, August 1998.

[Larsson 99] Patrik Larsson, "Power supply noise in future ICs: A crystal ball reading", *in Custom Integrated Circuits Proceedings of the IEEE*, pp. 467–474, San Diego, CA, USA, 16-19 May 1999.

[Larsson 01] Patrik Larsson, "Measurements and analysis of PLL jitter caused by digital switching noise", *IEEE Journal of Solid-State Circuits*, vol. 36, no. 7, pp. 1113–1119, July 2001.

[Lee 04] Han il Lee, Je-Kwang Cho, Kun-Seok Lee, In-Chul Hwang, Tae-Won Ahn, Kyung-Suc Nah, and Byeong-Ha Park, "A $\Sigma - \Delta$ fractional-N frequency synthesizer using a wide-band integrated VCO and a fast AFC technique for GSM/GPRS/WCDMA applications", *IEEE journal of solid-state circuits*, vol. 39, no. 7, pp. 1164–1169, July 2004.

[Liu 99] Tingyang Liu, J.D. Carothers, and W.T. Holman, "Active substrate coupling noise reduction method for ICs", *IEE Electronics Letters*, vol. 35, no. 4, pp. 1633–1634, September 1999.

[Liu 05] Junhua Liu, Huailin Liao, Ru Huang, and Xing Zhang, "Sigma-delta modulator with feedback dithering for RF fractional-N frequency synthesizer", *in IEEE Conference on Electron Devices and Solid-State Circuits*, pp. 137–139, December 2005.

[Lu 93] Fang Lu, Henry Samueli, Jiren Yuan, and Christen Svensson, "A 700-MHz 24-b pipelined accumulator in 1.2-μm CMOS for application as a numerically controlled oscillator", *IEEE journal of solid-state circuits*, vol. 28, no. 8, pp. 878–886, August 1993.

[Maget 02] Judith Maget, *Varactors and Inductors for Integrated RF Circuits in Standard MOS Technologies*, PhD thesis, Universität der Bundeswehr München, Neubiberg, December 2002.

[Marletta 05] Marco Marletta, Paolo Aliberti, Massimiliano Pulvirenti, Alberto Cavallaro, Steven Terryn, Pietro Filoramo, Raffaele Iardino, Vincenzo Spalma, and Salvatore Cosentino, "Fully integrated fractional PLL for bluetooth application", *IEEE Radio Frequency integrated Circuits Symposium*, pp. 557–560, 12-14 June 2005.

[Matsuya 87] Yasuyuki Matsuya, Kuniharu Uchimura, Atsushi Iwata, Tsutomu Kobayashi, Masayuki Ishikawa, and Takeshi Yoshitome, "A 16-bit oversampling A-to-D conversion technology using triple-integration noise shaping", *IEEE journal of solid-state circuits*, vol. sc-22, no. 6, pp. 921–929, December 1987.

[Maxim 07] Adrian Maxim, "A low reference spurs 15 GHz 0.13 μm CMOS frequency synthesizer using a fully-sampled feed-forward loop filter architecture", *IEEE journal of solid-state circuits*, vol. 42, no. 11, pp. 2503–2514, November 2007.

[Meninger 05] Scott Edward Meninger, *Low Phase Noise, High Bandwidth Frequency Synthesis Techniques*, PhD thesis, Department of

Electrical Engineering and Computer Science, Massachusetts Institute of Technology, May 2005.

[Miller 91] Brian M. Miller and Robert J. Conley, "A multiple modulator fractional divider", *IEEE Transactions on Instrumentation and Measurement*, vol. 40, no. 3, pp. 578–583, June 1991.

[Muer 02] Bram De Muer and Michel S. J. Steyaert, "A CMOS monolithic $\Sigma\Delta$-controlled fractional-N frequency synthesizer for DCS-1800", *IEEE journal of solid-state circuits*, vol. 37, no. 7, pp. 835–844, July 2002.

[Mutagi 96] R. N. Mutagi, "Pseudo noise sequences for engineers", *IEE Electronics and Communication Engineering Journal*, vol. 8, no. 2, pp. 79–87, April 1996.

[Norsworthy 92] Steven R. Norsworthy, "Effective dithering of sigma-delta modulators", *in IEEE International Symposium on Circuits and Systems*, pp. 1304–1307, San Diego, CA, USA, May 1992.

[Norsworthy 97] Steven R. Norsworthy, Richard Schreier, and Gabor C. Temes, *Delta-Sigma Data Converters: Theory, Design, and Simulation*, IEEE Press, Institute of Electrical and Electronics Engineers, Inc., 345 East 47th Street, New York, 1st edition, 1997.

[Owens 05] Brian E. Owens, Sirisha Adluri, Patrick Birrer, Robert Shreeve, Sasi Kumar Arunachalam, Kartikeya Mayaram, and Terri S. Fiez, "Simulation and measurement of supply and substrate noise in mixed-signal ICs", *IEEE journal of solid-state circuits*, vol. 40, no. 2, pp. 382–391, February 2005.

[Park 01] Chan-Hong Park, Ook Kim, and Beomsup Kim, "A 1.8-GHz self-calibrated phase-locked loop with precise I/Q matching", *IEEE journal of solid-state circuits*, vol. 36, no. 5, pp. 777–783, May 2001.

[Perrott 97] Michael H. Perrott, *Techniques for High Data Rate Modulation and Low Power Operation of Fractional-N Frequency Synthesizers*, PhD thesis, Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, September 1997.

[Pozar 90] David M. Pozar, *Microwave Engineering*, Addison-Wesley Publishing Company, first edition, 1990.

[Rhee 99] Woogeun Rhee, "Design of high-performance CMOS charge pumps in phase-locked loops", *in IEEE International Symposium on Circuits and Systems*, pp. 545–548, July 1999.

[Riley 93] Tom A. D. Riley, Miles A. Copeland, and Tad A. Kwasniewski, "Delta-sigma modulation in fractional-N frequency synthesis", *IEEE journal of solid-state circuits*, vol. 28, no. 5, pp. 553–559, May 1993.

[Roermund 04] Arthur van Roermund, Michiel Steyaert, and Johan H. Huijsing, *Analog Circuit Design*, Kluwer Academic Publishers, first edition, 2004.

[Säckinger 90] Eduard Säckinger and Walter Guggenbühl, "A high-swing, high-impedance MOS cascode circuit", *IEEE journal of solid-state circuits*, vol. 25, no. 1, pp. 289–298, February 1990.

[Sayed 02] Mohammed Sayed and Wael Badawy, "Performance analysis of single-bit full adder cells using 0.18, 0.25 and 0.35 CMOS technologies", *IEEE International Symposium on Circuits and Systems*, vol. 3, pp. III–559 – III–562, 2002.

[Schreier 04] Richard Schreier and Gabor C. Temes, *Understanding Delta-Sigma Data Converters*, IEEE Press, IEEE, Inc., 345 East 47th Street, New York, 1st edition, 2004.

[Shu 03] Keliu Shu, Edgar Sánchez-Sinencio, José Silva-Martínez, and Sherif H. K. Embabi, "A 2.4-GHz monolithic fractional-N frequency synthesizer with robust phase-switching prescaler and loop capacitance multiplier", *IEEE journal of solid-state circuits*, vol. 38, no. 6, pp. 866–874, June 2003.

[SMA06] *SMARTi 3G PMB5701: The First Single-Chip Multi-Band CMOS Radio Frequency (RF) UMTS Transceiver IC*, Infineon Technologies AG, 31 January 2006.

[Soens 05] Charlotte Soens, Geert Van der Plas, Piet Wambacq, Stéphane Donnay, and Maarten Kuijk, "Performance degradation of LC-tank VCOs by impact of digital switching noise in lightly doped substrates", *IEEE journal of solid-state circuits*, vol. 40, no. 7, pp. 1472–1481, July 2005.

[Solomko 06] Valentyn A. Solomko and Peter Weger, "11 GHz CMOS $\Sigma\Delta$ frequency synthesiser", *IEE Electronics Letters*, vol. 42, no. 21, pp. 1199–1200, October 2006.

[Stan 98] Mircea R. Stan, Alexandre F. Tenca, and Milos D. Ercegovac, "Long and fast up/down counters", *IEEE transactions on computers*, vol. 47, no. 7, pp. 722–735, July 1998.

[Stojanovic 99] Vladimir Stojanovic and Vojin G. Oklobdzija, "Comparative analysis of masterslave latches and flip-flops for high-performance and low-power systems", *IEEE journal of solid-state circuits*, vol. 34, no. 4, pp. 536–548, April 1999.

[Su 93] David K. Su, Marc J. Loinaz, Shoichi Masui, and Bruce A. Wooley, "Experimental results and modeling techniques for substrate noise in mixed-signal integrated circuits", *IEEE journal of solid-state circuits*, vol. 28, no. 4, pp. 420–430, April 1993.

[Sun 99] Lizhong Sun, Thieny Lepley, Franck Nozahic, Arnaud Bellissant, Tad A. Kwasniewski, and Bany Heim, "Reduced complexity, high performance digital delta-sigma modulator for fractional-N frequency synthesis", *Proceedings of the 1999 IEEE International Symposium on Circuits and Systems*, vol. 2, pp. 152–155, July 1999.

[Sze 81] S. M. Sze, *Physics of semiconductor devices*, John Wiley & Sons, New York, 2nd edition, 1981.

[Temporiti 04] Enrico Temporiti, Guido Albasini, Ivan Bietti, Rinaldo Castello, and Matteo Colombo, "A 700-kHz bandwidth $\Sigma\Delta$ fractional synthesizer with spurs compensation and linearization techniques for WCDMA applications", *IEEE journal of solid-state circuits*, vol. 39, no. 9, pp. 1446–1454, September 2004.

[Tiebout 04] Marc Tiebout, Christoph Sandner, Hans-Dieter Wohlmuth, Nicola Da Dalt, and Edwin Thaller, "A fully integrated 13 GHz $\Sigma\Delta$ fractional-N PLL in 0.13 μm CMOS", *in IEEE Solid-State Circuits Conference*, 15-19 February 2004.

[Tiebout 05] Marc Tiebout, Christoph Kienmayer, Ronald Thüringer, Christoph Sandner, Hans Dieter Wohlmuth, Mohit Berry, and Arpad Ludwig Scholtz, "17 GHz transceiver design in 0.13 μm CMOS", *in IEEE RFIC Symposium, Digest of Papers*, pp. 101–104, 2005.

[Unger 81] Stephen H. Unger, "Double-edge-triggered flip-flops", *IEEE Transactions on Computers*, vol. C-30, no. 6, pp. 447–451, June 1981.

[Vasylyev 06] Andriy Vasylyev, *Integrated RF Power Amplifier Design in Silicon-Based Technologies*, PhD thesis, Chair of Circuit Design, Brandenburg University of Technology Cottbus, Erich-Weinert-Str. 1, D-03046 Cottbus, Germany, July 2006.

[Vaucher 02] Cicero S. Vaucher, *Architectures for RF Frequency Synthesizers*, Kluwer Academic Publishers, Boston-Dordrecht-London, first edition, 2002.

[Winkler 05] Wolfgang Winkler, Johannes Borngräber, Bernd Heinemann, and Frank Herzel, "A fully integrated BiCMOS PLL for 60 GHz wireless applications", *in IEEE International Solid-State Circuits Conference*, pp. 406–407, San Francisco, CA, USA, February 2005.

[Xiaojian 07] Mao Xiaojian, Yang Huazhong, and Wang Hui, "Comparison of sigma-delta modulator for fractional-N PLL frequency synthesizer", *Journal of Electronics (China)*, vol. 24, no. 3, pp. 374–379, May 2007.

[Yang 06] Yu-Che Yang, Shih-An Yu, Yu-Hsuan Liu, Tao Wang, and Shey-Shi Lu, "A quantization noise suppression technique for $\Sigma\Delta$ fractional-N frequency synthesizers", *IEEE journal of solid-state circuits*, vol. 41, no. 11, pp. 2500–2511, November 2006.

[Ye 07] Zhipeng Ye and Michael Peter Kennedy, "Reduced complexity MASH delta-sigma modulator", *IEEE transactions on circuits and systems-II*, vol. 54, no. 8, pp. 725–729, August 2007.

[Yeh 04] Wen-Kuan Yeh, Shuo-Mao Chen, and Yean-Kuen Fang, "Substrate noise-coupling characterization and efficient suppression in CMOS technology", *IEEE Transactions on Electron Devices*, vol. 51, no. 5, pp. 817–819, May 2004.

[Young 94] Paul H. Young, *Electronic Communication Techniques*, Prentice Hall Inc., New York, first edition, 1994.

[Zhang 05] Pengfei Zhang et al., "A single-chip dual-band direct-conversion IEEE 802.11a/b/g WLAN transceiver in 0.18-μm CMOS", *IEEE journal of solid-state circuits*, vol. 40, no. 9, pp. 1932–1939, September 2005.