Multi-band Adaptive WLAN Receivers in 0.13 μm CMOS

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Abstract

This work demonstrates the design and implementation of a multi-band multi-standard WLAN system consisting of a 5 - 6 GHz receiver and a 24 GHz down-converter. The main challenges are high frequency, broadband, and adaptive operation, power consumption and high integration level. This thesis introduces a multi-standard adaptive receiver concept to fulfill those requirements.
The receivers are implemented in a standard 0.13 μm CMOS technology. A direct-conversion architecture for the 5 - 6 GHz band and a heterodyne architecture for a multi-band system are proposed. The most common receiver architectures are analyzed and the wave propagation effects are discussed. Then the most important receiver parameters are derived. Active and passive integrated components are investigated because understanding the device characteristic is a key requirement for a successful high frequency design. Finally, the multi-standard adaptive receiver concept is introduced. The choice of architecture, design and implementation of each of the receiver building blocks are discussed. The functionality of the 5 - 6 GHz receiver and the 24 GHz down-converter is demonstrated by the performance measurements.
The main achievements of this work include:

Firstly, a 5-6 GHz LNA integrated in 0.13 μm CMOS technology. The amplifier exhibits a gain of 16.5 dB, noise figure of 2.9 dB and 1 dB input compression point of -6.5 dBm at power consumption of 7.5 mW. The circuit features robust built-in input ESD protection.

Secondly, a 5-6 GHz zero-IF receiver with analog pre-processing features a noise figure of 3.8 dB at the conversion gain of 43.4 dB. The channel select filter corner frequency is tunable to 6.5, 10, 20 and 50 MHz. The implemented analog pre-processing loop allows to adopt the linearity of the receiver to the input signal level.

Thirdly, a 23-24 GHz tuned down-converter achieved the gain of 21.8 dB, noise figure of 6.8 dB and 1 dB input compression point of -16.7 dBm at power consumption of 58.5 mW.

Zusammenfassung

Diese Arbeit zeigt den Entwurf und die Implementierung eines Multi-Band Multi-Standard WLAN Systems bestehend aus einem 5 - 6 GHz Empfnger und einem 24 GHz Downconverter. Die wesentlichen Herausforderungen sind dabei die hohe Frequenz, die Breitbandigkeit, der adaptive Betrieb, der Energieverbrauch sowie der Integrationsgrad. In dieser Arbeit wird ein Multistandardempfängerkonzept eingeführt, welches diesen Herausforderungen gerecht wird.
Die Empfängerstufen sind in einer Standard 0.13 μm CMOS-Technologie implementiert. Eine homodyne Architektur für das 5 - 6 GHz Band und eine heterodyne Architektur fr das Multibandsystem werden vorgeschlagen. Mögliche Empfängerarchitekturen werden untersucht und ihre Übertragungseigenschaften analysiert. Darauf basierend werden die wichtigsten Parameter der Empfängerschaltung hergeleitet. Parallel dazu werden sowohl aktive als auch passive integrierte Bauelemente untersucht, da das Verständnis ihrer Eigenschaften eine Schlüsselrolle für den erfolgreichen HF-Schaltungsentwurf spielt. Darauf basierend wird das Konzept eines Multistandardempfängers entwickelt. Die Auswahl der Architektur, des Schaltungsentwurfes und der Implementierung jedes Empfängerblocks werden diskutiert. Die Funktionalität sowohl des 5 - 6 GHz Empfängers als auch des 24 GHz Downconverters werden durch entsprechende Messungen demonstriert.
Als wesentliche Ergebnisse dieser Arbeit wurden verwirklicht:

Erstens ein 5 - 6 GHz LNA, der in 0.13 μm CMOS Technologie integriert wurde. Dieser hat eine Verstärkung von 16,5 dB, eine Rauschzahl von 2,9 dB und der 1 dB Eingangskompressionspunkt liegt bei -6,5 dBm. Dabei ist die Leistungsaufnahme nur 7,5 mW. Die Schaltung besitzt robuste Eingangsschutzschaltungen.

Zweitens, wurde ein 5 - 6 GHz Zero-IF Empfänger mit analoger Vorverarbeitung und einer Rauschzahl von 3,8 dB bei eine Verstärkung von 43,4 dB realisiert. Die Grenzfrequenz der Kanalselektionsfilter ist auf 6,5,10,20 und 50 MHz abstimmbar. Die analoge Vorverarbeitungsstufe erlaubt es, die Linearität des Empfängers auf die Stärke des Eingangssignals abzustimmen.

Drittens, wurde ein 23 - 24 GHz Downconverter implementiert, der eine Verstärkung von 21,8 dB, eine Rauschzahl von 6,8 dB und einen 1 dB Eingangskompressionspunkt von -16,7 dBm bei einer Leistungsaufnahme von 58,5 mW aufweist.

Contents

List of Abbreviations

ADC	Analog-Digital Converter
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BSIM	Berkley Short-Channel IGFET Model
CLM	Channel-length Modulation
CMOS	Complementary Metal Oxide Semiconductor
CP	Compression Point
DC	Direct Current
DIBL	Drain Induced Barrier Lowering
DITS	Drain Induced Threshold Shift
DR	Dynamic Range
DSB	Double Side Band
ESD	Electrostatic Discharge
EVM	Error Vector Magnitude
FEM	Finite Element Method
FET	Field Effect Transistor
f_{max}	Maximum oscillation frequency in [Hz]
f_T	Transit frequency in [Hz]
HBM	Human Body Model
HF	High Frequency
I	Inphase Output
IC	Integrated Circuit
IP3	Third order intermodulation point
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate Frequency
IGFET	Isolated-Gate Field-Effect Transistor
IMD	Intermodulation Distortion
ISI	Intersymbol Interference
ISM	Industrial, Scientific and Medical frequency band
LAN	Local Area Network
LO	Local Oscillator
LNA	Low Noise Amplifier
LPF	Low Pass Filter
Mbps	Megabits per second
MDS	Minimum Detectable Signal
MIM	Metal-Insulator-Metal capacitor
MIMO	Multiple Input Multiple Output
MoM	Method of Moments
MOS	Metal Oxide Semiconductor

OFDM	Orthogonal Frequency Division Multiplexing
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
Q	Quadrature output
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuits
SCBE	Substrate CurrentInduced Body Effect
$SiGe$	Silicon-Germanium
SiO_2	Silicon-dioxide
SMA	Sub-miniature A connector
SNR	Signal-to-Noise Ratio
SSB	Single Side Band
WIGWAM	Wireless Gigabit with Advanced Multimedia
WLAN	Wireless Local Area Network

Notation

Throughout the thesis, signals (voltages and currents) are denoted as follows:

- Constant voltages and currents: with capital letters and capital indices (e.g. V_{SS})
- Total instantaneous voltages and currents: with capital letters and small indices (e.g. I_d)
- Small-signal voltages and currents and elements such as transconductance in small-signal equivalent circuits: with small letters and small indices (e.g. i_d, g_m)

Chapter 1

Introduction

The main advantage of wireless systems which is the mobility is becoming insufficient for the users as they require the same quality and service form wireless networks as offered by wired counterparts. Email, Internet access, video distribution, access to peripheral devices, and replacement of Ethernet network installations are example applications of wireless links (Figure 1.1). However, popular second-

Figure 1.1: WLAN environment.

(2G) and third-generation (3G) technologies do not fulfill those requirements. Even wireless short-range communication networks seem to be one generation

behind their wired counterparts, limiting their use as convenient replacement technology [Fettweis 05]. Therefore, there is a demand for a wireless short-range transmission technology capable of competing with wired LANs. However, the compatibility with the in-use wireless standards is essential because of their popularity and the number of applications. Current wireless systems use the ISM (Industrial, Scientific, Medical) radio bands at 2.4 GHz and 5 GHz. These bands are unlicensed and impose only a few rules concerning maximum output power and out of band emissions. There are also ISM bands allocated around 17 GHz, 24 GHz and 60 GHz which offer higher bandwidths allowing high data rates. In order to maximize the complexity and minimize the cost there is a big pressure to introduce multi-standard and multi-band solutions.

The competitiveness of new hardware products for wireless applications is predominantly defined by the manufacturing costs. This leads to the research on highly integrated solutions combining RF front-end and digital baseband parts on a single semiconductor die. Such ability of integration along with low manufacturing cost is only achievable with CMOS technology. Additionally, due to the small size of the devices, it allows a high integration level of complex digital circuitry and benefits from low power consumption in case of digital circuits.

Development work for mass production applications poses challenges for the design of RF integrated circuits (RFICs). To provide high yield the circuit performance must be stabilized against technology variations, temperature and supply voltage variations to provide high yield. This can be achieved by proper circuit design and biasing techniques. The power consumption is a very important issue which dominates in the design process. Finally, in consumer electronics applications, the size and cost of the components must be minimized. This leads to a high level of integration while minimizing the number of external components and chip area.
Next, the chips have to be mounted in a package to be protected form mechanical stress and the influence of the environment, and to ease the automatic mounting on printed circuit board (PCB). Additionally, the circuit interfaces must be protected by electrostatic discharge (ESD) protection structures to provide high reliability. The ESD protection in RF applications is very challenging since it strongly affects the performance of the circuits. It has to be considered in early phases of circuit design. Finally, scaling down transistors leads to lower supply voltage for RF circuits. This poses additional challenges on the realization of circuits with high dynamic range.

This work aims at the implementation of a fully integrated multi-band and multi-standard 5 - 6 GHz direct conversion receiver and a 24 GHz down-converter. The 5 - 6 GHz receiver includes a tunable RF front-end, and a tunable baseband filter. It is used as a backbone for the 24 GHz down-converter which is a band-extension of the whole system. The circuits are implemented in a standard 0.13μm CMOS technology and their performance was tested.

1.1 Current State-of-the-Art

Some of recently published results of fully integrated receivers for 5 GHz and 24 GHz frequency band are gathered in Table 1.1 and Table 1.2. Concerning the bandwidth and noise figure, the comparison of 5 GHz receivers shows that the results achieved here represent one of the leading positions among monolithically integrated receivers.

Table 1.1: Published state-of-the-art work for 5 GHz range.

	Bandwidth	Gain	NF	1 dB ICP	Level of integration	Technology
This work	5.1 - 6 GHz	43.4 dB	3.8 dB	-25.5 dBm	RX+BB Filter	CMOS
[Zhou 06]	5.1 - 5.9 GHz	76 dB	5.9 dB	-9 dBm	RX+BB Filter	SiGe
[Zito 06]	4.9 - 5.5 GHz	20 dB	4.7 dB	-20 dBm	RX	SiGe
[Chen 05]	5.1 - 5.4 GHz	28.2 dB	6.4 dB	-19 dBm	RX	CMOS
[Samavati 00]	5 - 5.4 GHz	12 dB	5.2 dB	-14 dBm	RX	CMOS

Table 1.2 shows that a standard CMOS technology is suitable for applications beyond 20 GHz. The results obtained for the implemented in this work circuits clearly can compete with SiGe BiCMOS counterparts.

Table 1.2: Published state-of-the-art work for 24 GHz range.

	Bandwidth	Gain	NF	1 dB ICP	Technology
This work	22.7 - 24.5 GHz	21.5 dB	7 dB	-17 dBm	0.13 μm CMOS
[Gresham 06]	22 - 26 GHz	45 dB	7.8 dB	n/a	Atmel's SiGe 2RF
[Sonmez 05]	23.4 - 24.4 GHz	33 dB	n/a	-27 dBm	0.8 μm SiGe BiCMOS
[Guan 04,b]	23.5 - 24 GHz	43 dB	7.4 dB	-27 dBm	0.18 μm SiGe BiCMOS
[Guan 04,a]	21.5 - 22.2 GHz	27.5 dB	7.7 dB	-23 dBm	0.18 μm CMOS

Chapter 2

Wireless Receivers Fundamentals

2.1 Propagation Effects

The electromagnetic wave propagated in a radio communication channel is subject to a variety of effects. Frequency, distance, terrain, objects in the path of the wave, and reflections all can alter the power of the wave at any point in space. Understanding how the propagated wave is affected in real environment is critical to the design of any radio-based application.

2.1.1 Free Space Propagation and Path Loss

Let us consider an idealized radio system link where there is no reflection, scattering or diffraction along the path between the transmitter and receiver. The relation between the received power P_R and the transmitted power P_T is given by Friis equation

$$\frac{P_R}{P_T} = G_T G_R L_P. \tag{2.1}$$

where L_P is the path loss, G_T and G_R are the transmit and receive antenna gains, respectively.

The path loss L_P in free space is given by

$$L_P = \left(\frac{\lambda}{4\pi d}\right)^2 = \left(\frac{c}{4\pi df}\right)^2. \tag{2.2}$$

where d is the distance between transmitter and receiver, f the frequency, λ the wavelength and c is the speed of light in vacuum ($3 \cdot 10^8\, m/s$).

In practice, the Friis formula can be used when there is essentially a single line-of-sight path between the transmitter and receiver as illustrated in Figure 2.1. This requires that at least one of the link antennas has a narrow beamwidth, which is true in case of point-to-point radio links, satellite-to-satellite links or earth-to-satellite links.

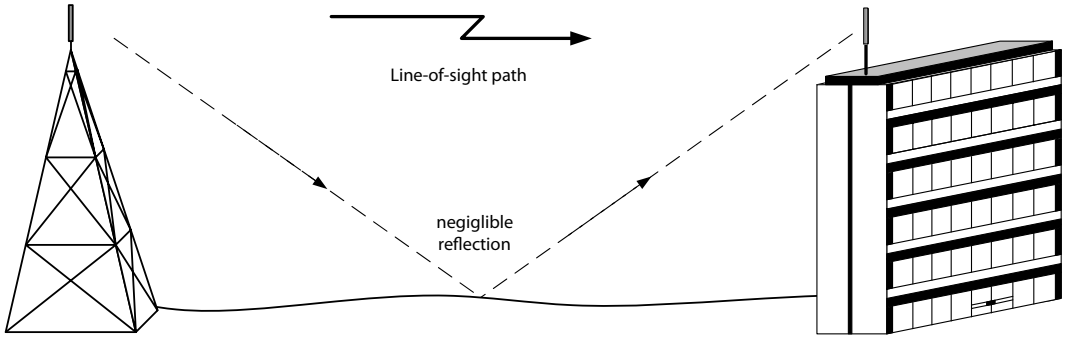


Figure 2.1: A point-to-point radio link with a single line-of-sight propagation path.

2.1.2 Multipath and Fading

Applications like wireless LAN or mobile communication systems serve end users which are located among a mix of obstacles and reflective objects as shown in Figure 2.2. The reflections, scattering and diffractions can create more than a single path between the transmitter and receiver. In worst-case, there may be no line-of-sight path but the communication will still be possible. The total received signal at the receiver will experience various degrees of destructive or constructive interferences due to the different phase delays caused by different signal paths. Such fluctuations of the received signal at the antenna are referred as fading. Besides amplitude variations and variable signal delays caused by different propagation paths, fading can also involve frequency modulation due to Doppler effects caused by moving objects or antenna.

2.1.3 Diversity

Diversity techniques are used to increase the communication reliability in a multipath environment. The multipath effect leading to signal cancellation or strengthening is dependent on transmitter and receiver spatial positions, on frequency and on polarity. Using these parameters, the following diversity techniques can be distinguished:

- **Spatial Diversity**

  In this technique, multiple receiver antennas are strategically placed at different locations. This is one of the most common diversity technique and there are two different methods to implement it, as illustrated in Figure 2.3. One method is to switch between multiple antennas. That requires the receiver to test the signal at each antenna and then make a decision which one to use. The other method uses multiple receiver paths with their own an-

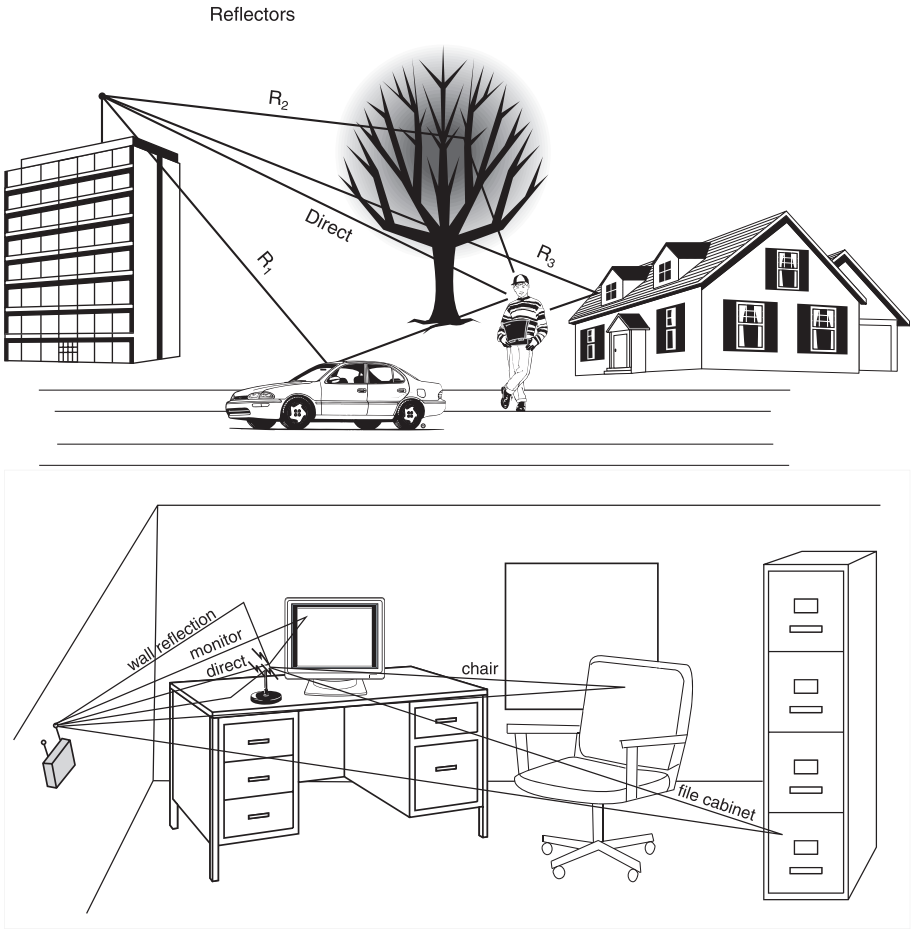


Figure 2.2: Typical outdoor and indoor environments for wireless communication, source [Olexa 05].

tennas. In this case the signals are simultaneously delivered to the receiver back-end where the choice of the best signal is done.

- **Frequency Diversity**

  This diversity technique uses a single receiver antenna but the signal is transmitted over two or more frequency separated channels. As in the case of spatial diversity, the strongest signal is chosen improving an average signal-to-noise ratio of the received signal. The required frequency separation between the channels depends on the path lengths or signal delays. The larger the difference in path lengths, the smaller the required frequency difference.

- **Polarization Diversity**

  Antennas with orthogonal polarization can provide two independently fading channels. The direction of polarization of a radio wave can be changed

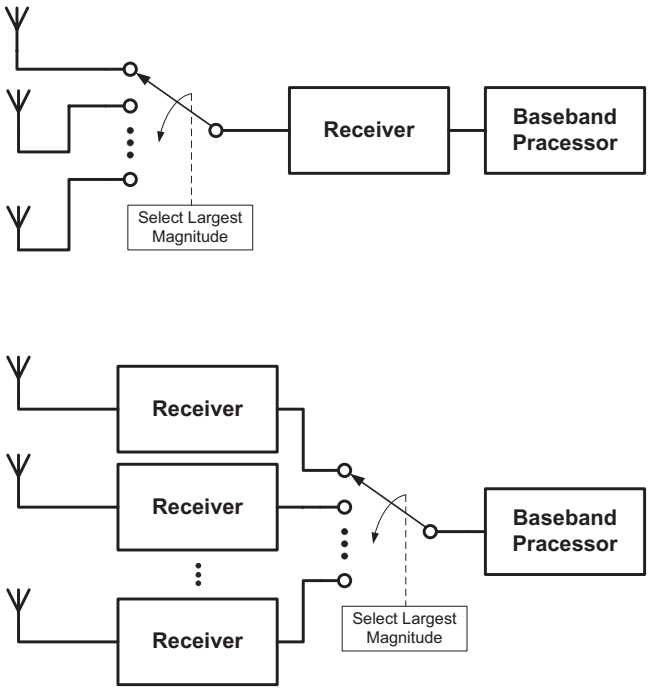


Figure 2.3: Spatial diversity techniques.

due to reflections and this feature can be used to create two separate signal channels. Thus, cross-polarized antennas can be used only at the receiver. Polarization diversity may be particularly advantageous in a portable handheld transmitter, since the orientation of its antenna is not strictly defined ([Bensky 00]).
Polarization diversity is limited to the usage of only two channels and the degree of independence of each channel will be usually less than in the two other cases.

2.1.4 Equalization

Equalization of radio communication channels was developed to reduce intersymbol interference (ISI). As a result of multipath and other channel distortions, tails of prior symbols or precursors of symbols yet to come cause intersymbol interference that reduces or eliminates tolerance to noise. To reduce ISI in a mobile environment, adaptive equalization is used to track the time-varying characteristics of the channel. Typically, a known training sequence is transmitted to characterize the channel. The received information is then manipulated to calculate and set the proper filter coefficients for equalization in the receiver back-end. The data is transmitted following the training sequence while the received data is corrected by the equalizer. In an adaptive equalizer, the filter coefficients of the equalizer are constantly optimized to compensate the changing radio channel.

2.2 Receiver Architectures

Typical radio receivers convert the modulated radio frequency (RF) signal to an appropriate intermediate (IF) frequency by multiplying (or mixing) it with a local oscillator (LO) signal. The down-converted signal can be either demodulated in analog domain or converted to digital domain by means of an analog-to-digital converter (ADC) and then demodulated. The receiver is also required to restore the received signal to a level near its original baseband value. In order to fulfill this requirement the receiver should provide high gain, which should be spread over the RF, IF and baseband stages to avoid instabilities and possible oscillation. Selectivity of the receiver defines its ability to receive the desired signal while rejecting adjacent channels, image frequencies and interference. This can be accomplished by using a narrow bandpass filter at the RF stage of the receiver and a channel selection filter before detection.

2.2.1 Heterodyne Architecture

The heterodyne receiver is a commonly used architecture for radio communication. The block diagram of the receiver architecture and frequency translation scheme are shown in Figure 2.4 and Figure 2.5. The received signal from the antenna is filtered by a bandpass filter, which suppresses unwanted signals lying outside the RF band of interest. A LNA amplifies the signal with the minimized noise contribution. The mixer multiplies the RF signal with the local oscillator (LO) signal. The channel selection is performed by a filter at IF frequency and further blocks carry out the demodulation or detection to retrieve the desired information.

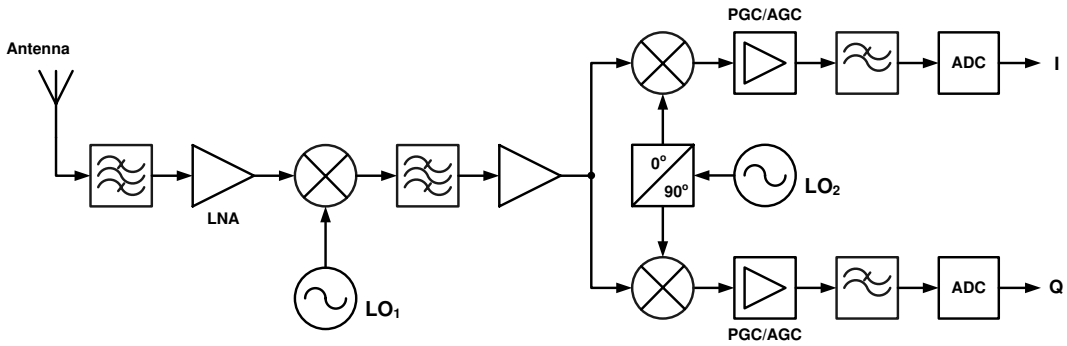


Figure 2.4: Block diagram of a heterodyne I/Q receiver.

One major issue in heterodyne receivers is the suppression of unwanted image signals. The most common approach to suppressing the image is through the use of a image-reject filter placed before the mixer. Such a filter can only be realized when the IF is high enough because in this case the wanted signal is far

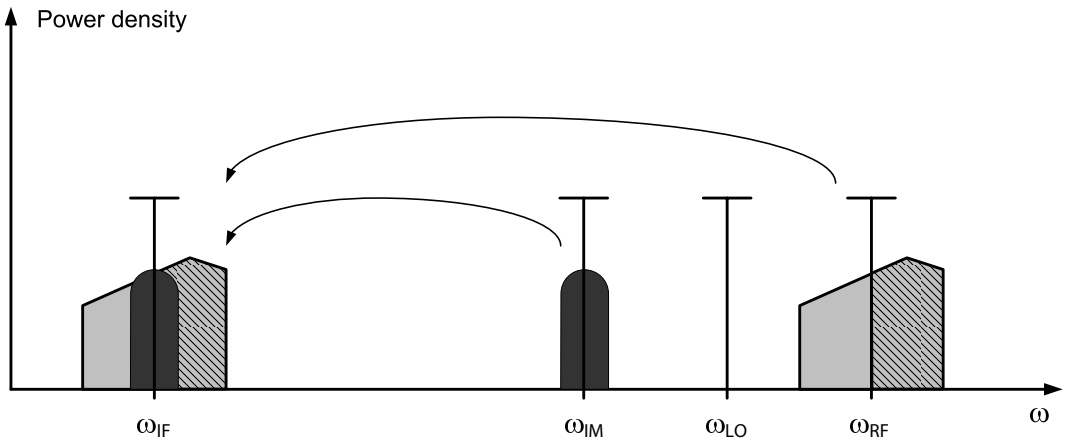


Figure 2.5: Frequency scheme in heterodyne architecture.

away from the mirror frequency. A high IF leads to substantial rejection of the image but requires high selectivity in the channel-select filter. In the case of low IF, the requirements for channel-select filter are more relaxed, however, a high-selectivity of the image filter is required. The HF filters are realized as discrete external components, rising the overall production and assembly costs.

2.2.2 Sliding-IF Receivers

A sliding IF receiver employs one local oscillator for both mixing stages. In this case, in contrast to a standard heterodyne architecture, the IF is no longer fixed and the signal frequency after first down-conversion is sliding. A block diagram of a receiver using the sliding IF architecture is presented in Figure 2.6.

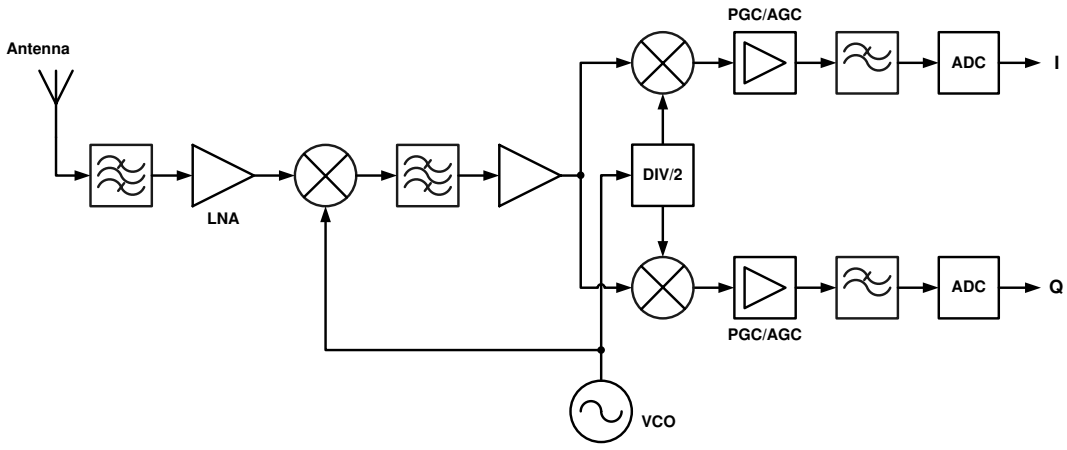


Figure 2.6: Block diagram of a sliding IF I/Q receiver.

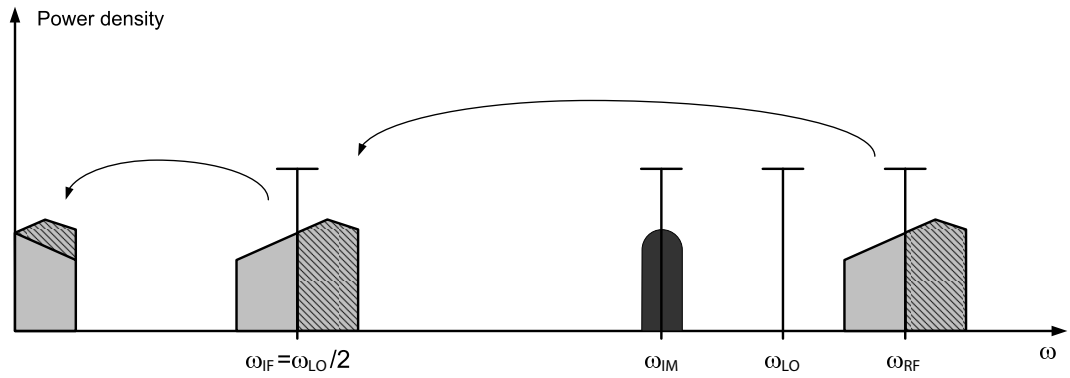


Figure 2.7: Frequency scheme in a sliding IF I/Q receiver.

The block diagram shows a receiver architecture implemented by [Chen 03], where the chosen division ratio is 2:1. In general the division ratio depends on the frequency planning and can have arbitrary ratio. The lack of the second LO increases the integrity of the system. The presence of two conversion steps enables separate optimization for gain and flicker noise of the first and the second mixers respectively.

2.2.3 Direct Conversion Receivers

A direct conversion or zero-IF receiver is an alternative to the heterodyne one. It allows the elimination of the IF stages be setting the local oscillator signal to the same frequency as the desired RF signal. In this case we obtain a direct conversion form RF to baseband as illustrated in Figure 2.9. The direct conversion receiver architecture is illustrated in Figure 2.8.

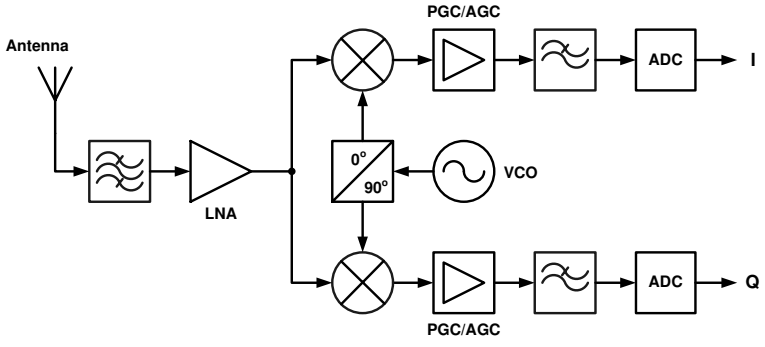


Figure 2.8: Block diagram of a direct conversion I/Q receiver.

In order to demodulate frequency and phase-modulated signals the receiver must provide quadrature outputs since the two sides of spectra carry the information.

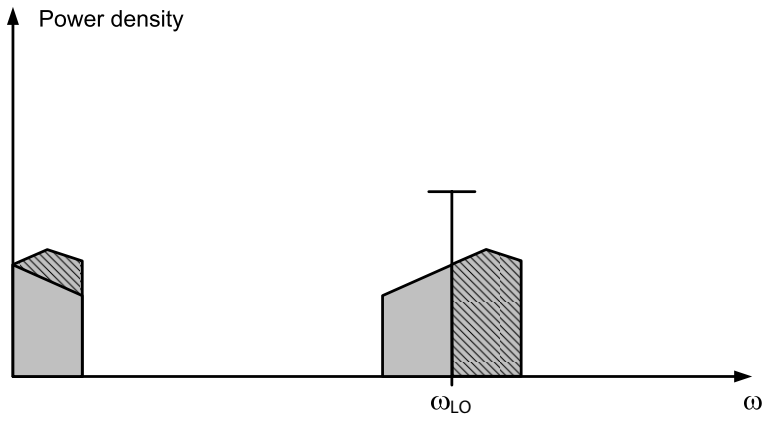


Figure 2.9: Frequency scheme in a direct conversion I/Q receiver.

The main advantage of the zero-IF receiver is that by shifting the IF to zero, the need for any image-reject filter is eliminated. A pair of channel-select filters can be realized as active, on-chip circuits making the complete integration of the receiver possible. The zero-IF receiver does suffer from some limitations. These are mainly associated with unwanted DC offsets and second-order intermodulation products generated in the mixers which occupy the same frequency band as the wanted signal. They can seriously desensitize the receiver and are particularly troublesome in narrow-band applications. Another important problem appearing in zero-IF receivers is the flicker noise. Since the IF is at zero frequency, the mixer and other stages in the baseband must be optimized in order to minimize the flicker noise.

2.3 Receiver Performance

To guarantee a sufficient performance in real world scenarios the receiver has to fulfill the requirements defined during standardization process. A set of parameters defining the performance of the receiver is presented in the following subsections.

2.3.1 Noise Figure and Sensitivity

Noise figure quantifies the noise performance of a component or a system. The noise factor of a two-port network is given by:

$$F = \frac{SNR_{in}}{SNR_{out}}, \tag{2.3}$$

where SNR_{in} and SNR_{out} are the signal-to-noise ratios measured at the input and at the output. The noise figure NF is expressed in decibels and defined as:

$$NF = 10 \log \frac{SNR_{in}}{SNR_{out}} = 10 \log F. \tag{2.4}$$

A receiver is a system of cascaded n elements. If each component is characterized in terms of noise factor and gain, the overall noise factor of a cascaded system is defined as:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \cdots G_{n-1}}, \tag{2.5}$$

where the subscripts refer to consecutive stages numbered from the input to the output.

Table 2.1: Receiver sensitivity requirements for a 5 GHz WLAN system

Data rate (Mbit/s)	Minimum sensitivity (dBm)
6	-82
9	-81
12	-79
18	-77
24	-74
36	-70
48	-66
54	-65

The sensitivity of a receiver is defined as the minimum signal power level that the system can detect with sufficient signal-to-noise ratio. It depends on the thermal

noise power from the input resistance of the signal source, the noise performance of the receiver expressed as noise figure, the bandwidth of the receiver and the required signal-to-noise ratio. The sensitivity is given by [Razavi 98]:

$$P_{min}|_{dBm} = P_{RS}|_{dBm/Hz} + NF|_{dB} + 10\log\ B + SNR_{min}|_{dB}, \tag{2.6}$$

where for conjugate match at the input, the input source noise power is

$$P_{RS} = 10\log(kT) = -173.87\, dBm/Hz. \tag{2.7}$$

In case of digital communication systems bit-error-rate (BER) is used to measure the reception quality. The BER is defined as the percentage of bits that are affected by errors relative to the bits received in the transmission. Hence, in case of an analog part of a digital receiver the BER has to be mapped onto the equivalent minimum SNR.Table 2.1 presents the minimum sensitivity requirements of 802.11a standard for different data rates [IEEE 99].

2.3.2 Linearity and Desensitisation

The linearity of a receiver is expressed in terms of 1 dB compression point (CP). It is defined as the input level signal that causes small-signal gain to drop by 1 dB. 1 dB CP limits the dynamic range (DR) of the receiver.The DR can be defined as the difference between the 1 dB CP and the minimum input detectable signal (MDS) level (Figure 2.10):

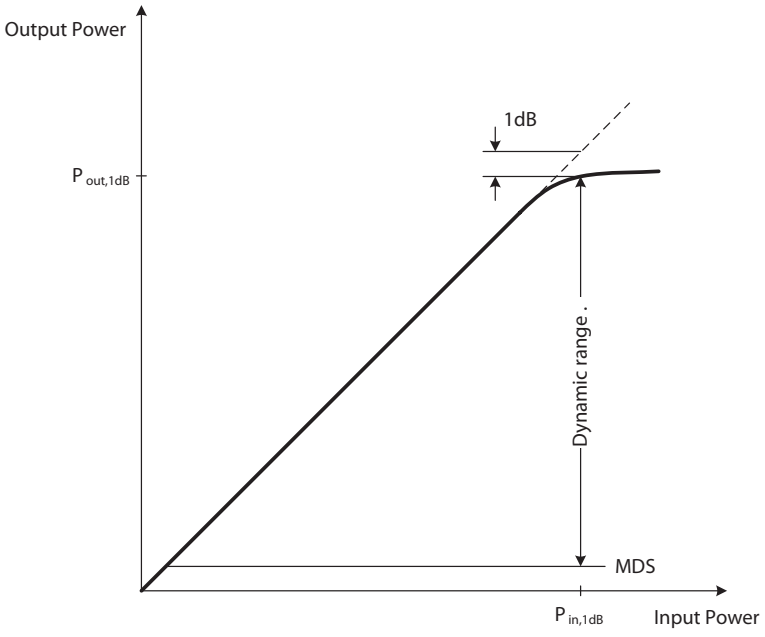


Figure 2.10: Definition of 1 dB compression point.

$$DR = P_{1dB} - MDS. \tag{2.8}$$

Large unwanted signals may appear at the input of the receiver along with a weak desired signal which has to be processed. The large blocker tends to reduce the gain of the receiver and the weak signal experience a vanishingly small gain. This effect is called *desensitisation*. The blocking signals that the receiver has to cope with are given by the standard, in case 5 GHz WLAN system they are shown in Figure 2.11.

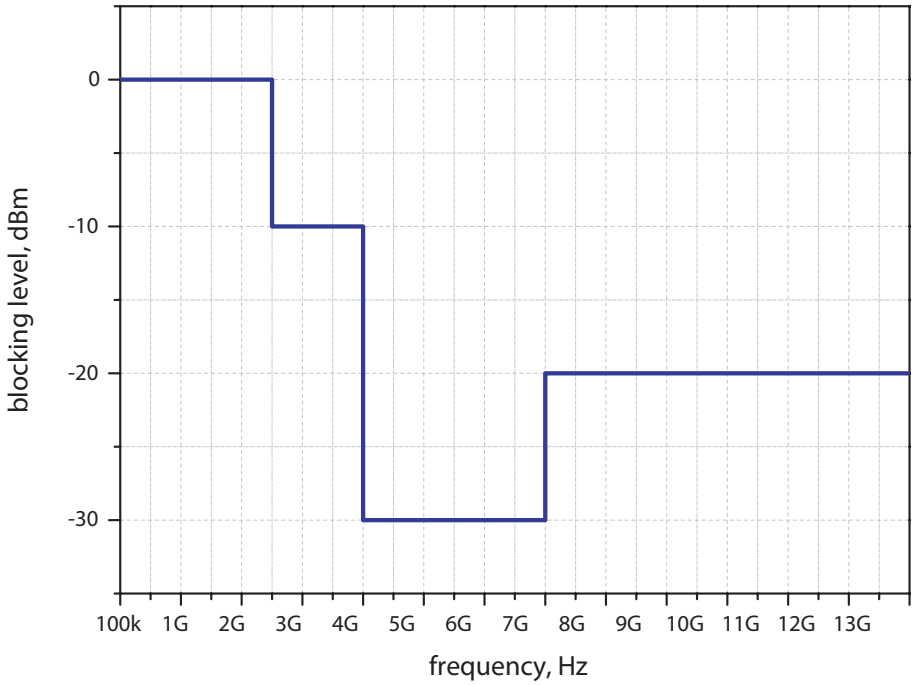


Figure 2.11: The allowed blocking signals for a 5 GHz WLAN system.

2.3.3 Intermodulation Distortion

When two signals with different frequencies are applied to a nonlinear system, the output exhibits some components that are not harmonics of the input frequencies [Razavi 98]. This phenomenon is known as *intermodulation* (IM) and arises from multiplication of the two signals when their sum is raised to a power greater than unity. Assuming a simple time-invariant memoryless system a Taylor-series representation can be used:

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t), \tag{2.9}$$

and using an input signal consisting of two sinusoidal signals with different frequencies and amplitudes,

$$x(t) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t \tag{2.10}$$

the response of the system can be written as:

$$\begin{aligned} y(t) &= \alpha_1(A_1\cos\omega_1 t + A_2\cos\omega_2 t) + \alpha_2(A_1\cos\omega_1 t + A_2\cos\omega_2 t)^2 \\ &+ \alpha_3(A_1\cos\omega_1 t + A_2\cos\omega_2 t)^3 \end{aligned} \tag{2.11}$$

Expanding the left side of (2.11) and discarding dc terms and harmonics, we obtain the following intermodulation products:

$$\omega = \omega_1 \pm \omega_2 : \alpha_2 A_1 A_2\cos(\omega_1+\omega_2)t + \alpha_2 A_1 A_2\cos(\omega_1-\omega_2)t \tag{2.12}$$

$$= 2\omega_1 \pm \omega_2 : \frac{3\alpha_3 A_1^2 A_2}{4}\cos(2\omega_1+\omega_2)t + \frac{3\alpha_3 A_1^2 A_2}{4}\cos(2\omega_1-\omega_2)t \tag{2.13}$$

$$= 2\omega_2 \pm \omega_1 : \frac{3\alpha_3 A_1 A_2^2}{4}\cos(2\omega_2+\omega_1)t + \frac{3\alpha_3 A_1 A_2^2}{4}\cos(2\omega_2-\omega_1)t \tag{2.14}$$

and these fundamental components

$$\omega = \omega_1, \omega_2 : \left(\alpha_1 A_1 + \frac{3}{4}\alpha_3 A_1^3 + \frac{3}{2}\alpha_3 A_1 A_2^2\right)\cos\omega_1 t \tag{2.15}$$

$$+ \left(\alpha_1 A_2 + \frac{3}{4}\alpha_3 A_2^3 + \frac{3}{2}\alpha_3 A_2 A_1^2\right)\cos\omega_2 t \tag{2.16}$$

The IM products are illustrated in Figure 2.12. If the difference between ω_1 and ω_2 is small the intermodulation products appear in the vicinity of ω_1 and ω_2, thus distorting the useful signal.

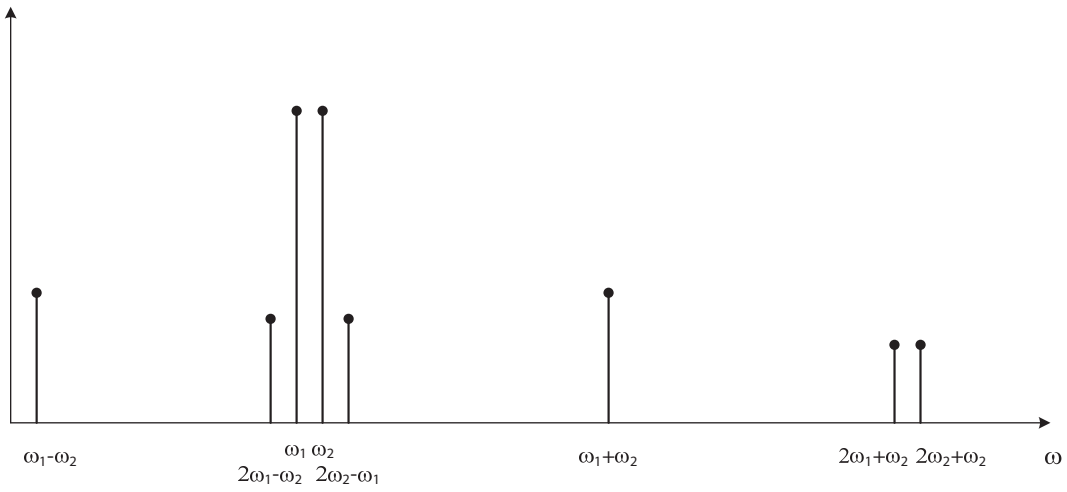


Figure 2.12: Output spectrum of two-tone analysis, showing intermodulation products of a nonlinear system.

The corruption of the signal due to third-order intermodulation of two nearby interferers is characterized by *third intercept point* (IP_3). This parameter is measured by a two-tone test in which $A_1 = A_2 = A$ is chosen to be sufficiently small

so that the higher-order nonlinear terms are negligible and the gain is relatively constant and equal to α_1.From (2.12), (2.13) and (2.14) with increasing A, the fundamentals increase in proportion to A, whereas the third-order IM products increase in proportion to A^3.The third-order intercept point is defined to be at the interception of the two lines as illustrated in Figure 2.13.

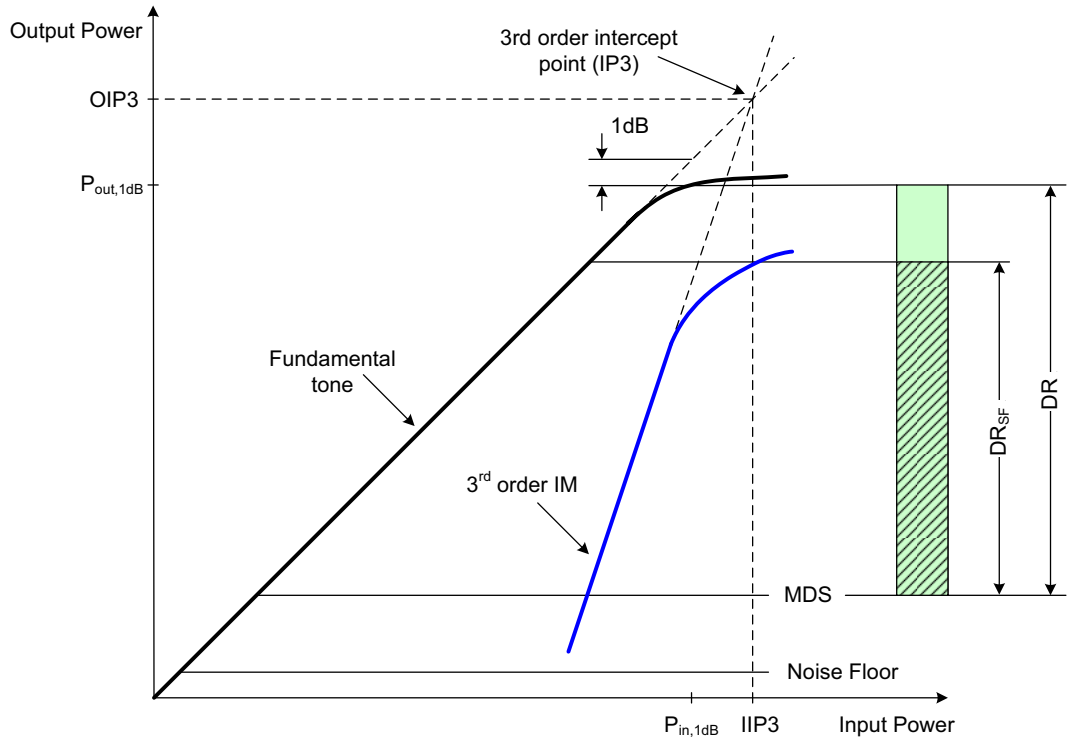


Figure 2.13: Graphical definition of IP3.

The IP_3 defines the *spurious-free dynamic range* (DR_{SF})which characterizes the receiver with more than one signal applied to the input. The DR_{SF} is given by:

$$DR_{SF} = \frac{2}{3}\left(IP3 - MDS\right), \tag{2.17}$$

where MDS is the minimum detectable signal.
The third order intercept point of a RF system which consists of cascaded blocks can be determined from:

$$IIP_3 = \frac{1}{\frac{1}{IIP_{3,1}} + \frac{G_1}{IIP_{3,2}} + \cdots + \frac{G_1 \cdots G_n}{IIP_n}}, \tag{2.18}$$

where $IIP_{3,x}$ and G_x denote the input referred IP_3 and gain of the cascaded stages.

2.3.4 I/Q Mismatch

Most modern wireless systems use quadrature modulations. The receiver is then required to separate I and Q signals using quadrature mixing. This is usually accomplished by shifting the LO signal as shown in Figure 2.14. The errors in the nominal 90^o phase shift and mismatches between the amplitudes of I and Q signals corrupt the down-converted signal constellation.

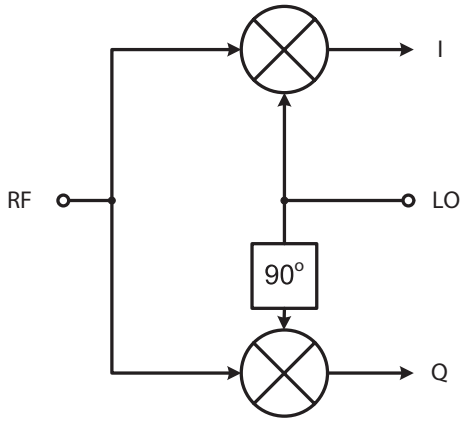


Figure 2.14: Quadrature generation in LO path.

For a received signal defined as $V_{in}(t) = I(t)\cos\omega_C(t) + Q(t)\sin\omega_C(t)$, and amplitude and quadrature phase imbalance of ϵ and θ, respectively,the baseband I and Q voltages are given by [Laskar 04]:

$$V_I = I(t)\left(1+\frac{\epsilon}{2}\right)\cos\left(\frac{\theta}{2}\right) - Q(t)\left(1+\frac{\epsilon}{2}\right)\sin\left(\frac{\theta}{2}\right) \tag{2.19}$$

$$V_Q = I(t)\left(1-\frac{\epsilon}{2}\right)\sin\left(\frac{\theta}{2}\right) + Q(t)\left(1-\frac{\epsilon}{2}\right)\cos\left(\frac{\theta}{2}\right) \tag{2.20}$$

Figure 2.15 shows the resulting QPSK signal constellation affected by gain and phase error. Table 2.2 presents the I/Q mismatch requirements for various modulation schemes defined for 802.11a standard [IEEE 99].

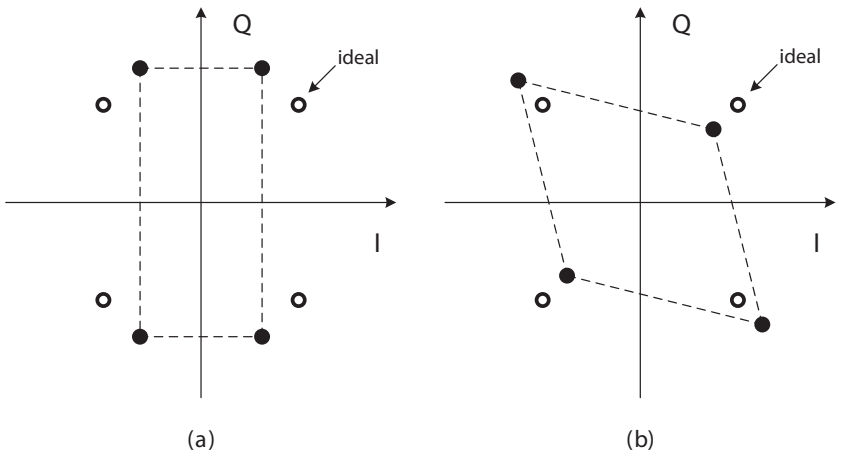


Figure 2.15: Effect of I/Q mismatch on QPSK signal constellation: (a) gain error, (b) phase error.

Table 2.2: I/Q mismatch requirements for various modulation schemes in 802.11a

Data rate (Mbps)	Modulation scheme	Gain imbalance, as phase imbalance = 0	Phase imbalance, as gain imbalance = 0
12	QPSK	≤ 1.90	≤ 25.62
18	QPSK	≤ 1.36	≤ 18.14
24	16-QAM	≤ 0.97	≤ 12.84
36	16-QAM	≤ 0.69	≤ 9.09
48	64-QAM	≤ 0.49	≤ 6.43
54	64-QAM	≤ 0.34	≤ 4.56

2.3.5 DC Offset

Since in a zero-IF topology the down-converted band extends to zero frequency, extraneous DC voltages can corrupt the signal and while propagating through the baseband circuitry they can saturate the following stages. The DC offsets are mostly generated through self-mixing the LO signal and mismatch in mixers [Abidi 95], [Crols 98].
In direct conversion-receivers, the mixer is immediately followed by LPFs and a chain of high-gain direct-coupled amplifiers that can amplify small levels of DC offset and saturate the following stages. The sensitivity of the receiver can be therefore limited by the DC offset component of the mixer output. The DC offset consists of two components, a time varying and a constant offset. The constant component origins from mismatch between mixer components while the time varying component arises due to the self-mixing of the LO signal caused by *LO leakage*(see Figure 2.16). The leakage is caused by imperfect isolation between the LO and the RF input of the mixer. In addition, the LO leakage and even the LO radiation can reach the LNA and propagate through the front-end. These

signals may be amplified prior to arriving at the mixer and due to the self mixing generate a relatively large DC component at the mixer output. The level of this DC offset, which is dependent on the time-varying load of the antenna, can also vary with time [Laskar 04]. It is obvious that homodyne receivers require some

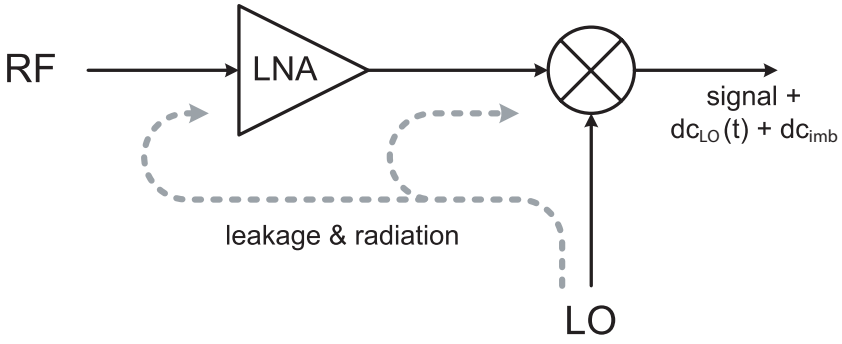


Figure 2.16: Generation of DC offsets.

means of DC offset cancellation. One of the simplest ways would be to use AC coupling. However, the spectrum of many commonly used modulated signals carry substantial information near DC, and it would require the usage of very large capacitors impossible to be integrated as a part of analog circuits [Crols 98]. Many DC offset cancellation analog and digital techniques have been reported recently. Most of the analog techniques require large off-chip capacitors and the digital techniques employ complex digital circuitry typically implemented in a separate chip.

Chapter 3

Technologies for Wireless Systems Integration

3.1 CMOS Technology

CMOS technologies are very attractive for wireless applications due to the possibility of integrating the digital base-band part together with RF front-end on a single chip. The 0.13 μm C11N RF of Infineon fabrication process was used within this work. This technology offers six metalization layers, Metal-Insulator-Metal (MIM) capacitors, and the minimum drawing length of a transistor of 0.12 μm.

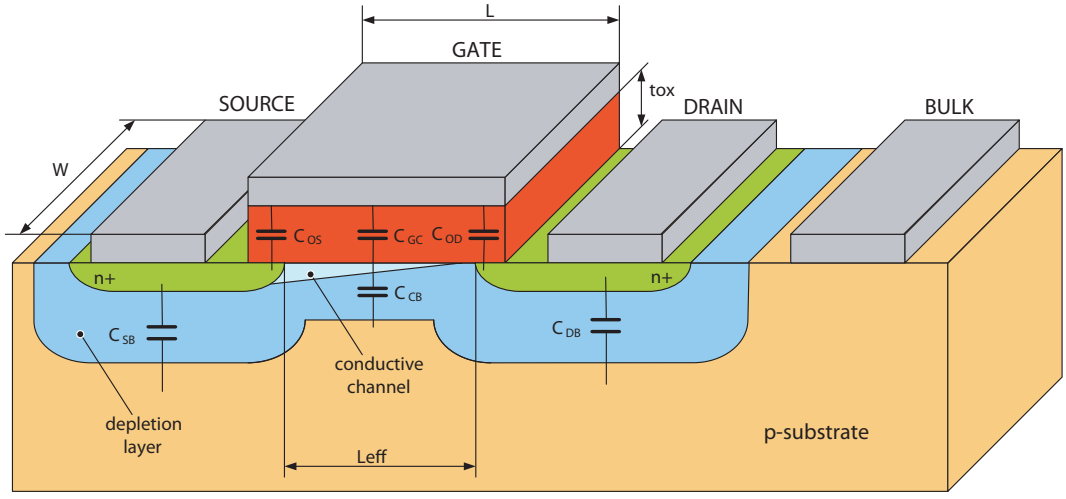


Figure 3.1: The cross section of a N-channel MOS transistor with parasitic capacitances.

3.1.1 MOS Transistors

The C11N RF process offers transistors with the minimum drawing length of 0.12 μm. Additionally the transistors can have different threshold voltages (low V_t, regular V_t and high V_t).

A typical cross section of a NMOS transistor is shown in Figure 3.1.

Transistor modeling

The modeling of transistors produced in modern CMOS technologies requires taking into account many novel effects. One of commonly used MOS transistor models is Berkeley Short-Channel IGFET Model, referred as BSIM. This model places less emphasis on the exact physical formulation of the device, but instead uses empirical parameters and polynomial equations to handle physical effects. BSIM model has been improved over recent years leading to the latest release known as BSIM4 [Liu 01].

The BSIM model provides different equivalent circuit configurations depending on the control parameters. The large-signal BSIM4 equivalent circuit shown in Figure 3.2 applies to the following parameter setup: *rdsMod*=0, *rgateMod*=0 (no gate resistance), *rbodyMod*=0 (no substrate network). In case when *rdsMod*=0 and $R_{DS}\neq 0$ the series drain and source resistance components are embedded in the I-V equation instead of physical resistance components in the equivalent model. The impact of the source and drain resistance is modeled in DC but not in AC and noise simulation in this case [Ytterdal 03].

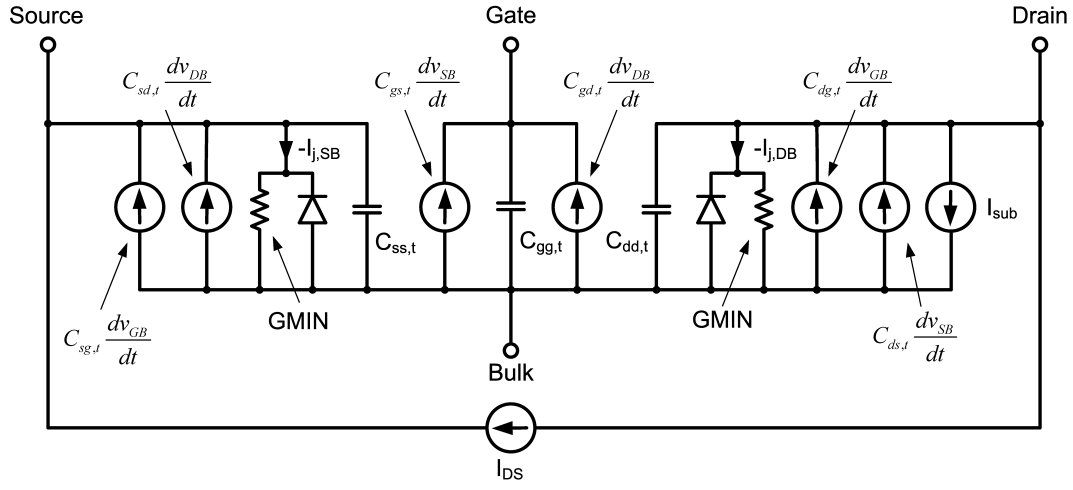


Figure 3.2: BSIM4 large-signal equivalent circuit (*rdsMod*=0, *rgateMod*=0, *rbodyMod*=0) .

The complete single equation channel current model including the contributions

of velocity saturation, channel-length modulation (CML), drain induced barrier lowering (DIBL), substrate currentinduced body effect (SCBE) to the channel current and conductance, and drain induced threshold shift (DITS) caused by pocket implantation is given by [Liu 01]:

$$\begin{aligned} I_{ds} &= \frac{I_{ds0}}{1+\frac{R_{DS}I_{ds0}}{V_{dseff}}}\left[1+\frac{1}{C_{CLM}}\ln\left(\frac{V_A}{V_{ASAT}}\right)\right]\left(1+\frac{V_{ds}-V_{dseff}}{V_{ADIBL}}\right) \\ &\times \left(1+\frac{V_{ds}-V_{dseff}}{V_{ADITS}}\right)\left(1+\frac{V_{ds}-V_{dseff}}{V_{ASCBE}}\right), \end{aligned} \tag{3.1}$$

where

$$V_A = V_{SAT} + V_{ACLM}. \tag{3.2}$$

The current I_{ds0} in (3.1) is the channel current for an intrinsic device (without including the source/drain resistance) in the regions from strong inversion to sub-threshold which is given as:

$$I_{ds0} = \frac{W_{eff}\cdot\mu_{eff}\cdot C'_{ox,IV}\cdot V_{gsteff}\cdot V_{dseff}}{L_{eff}\left(1+\frac{\mu_{eff}V_{dseff}}{2VSATL_{eff}}\right)}\left(1-\frac{V_dseff}{2V_b}\right), \tag{3.3}$$

where

$$V_b = \frac{V_{gsteff}+2kT/q}{A_{bulk}}. \tag{3.4}$$

The substrate current in BSIM4 model is defined as:

$$\begin{aligned} I_{sub} &= \left(\frac{ALPHA0}{L_{eff}}+ALPHA1\right)(V_{ds}-V_{dseff})\exp\left[-\frac{BETA0}{V_{ds}-V_{dseff}}\right] \\ &\times \frac{I_{ds0}}{1+\frac{R_{DS}I_{ds0}}{V_{dseff}}}\left(1+\frac{1}{C_{CLM}\ln\frac{V_A}{V_{ASAT}}}\right)\left(1+\frac{V_{ds}-V_{dseff}}{V_{ADIBL}}\right) \\ &\times \left(1+\frac{V_{ds}-V_{dseff}}{V_{ADITS}}\right), \end{aligned} \tag{3.5}$$

Gate resistance modeling

BSIM4 provides several gate resistance models, introducing the selector *RGATEMOD* to choose between them. When *RGATEMOD*=1 a gate resistance is added to the intrinsic model of the transistor. The value of the resistance is calculated as:

$$R_{Geltd} = \frac{RSHG\left(XGW+\frac{W_{eff,CJ}}{3NGCON}\right)}{NGCON\,(L-XGL)\,NF}, \tag{3.6}$$

where *RSHG* denotes the sheet resistance of the gate polysilicon. *NGCON* is the number of gate contacts for each finger (the gate finger can be contacted either at one or both sides as illustrated in Figure 3.3). *XGW* defines the distance between

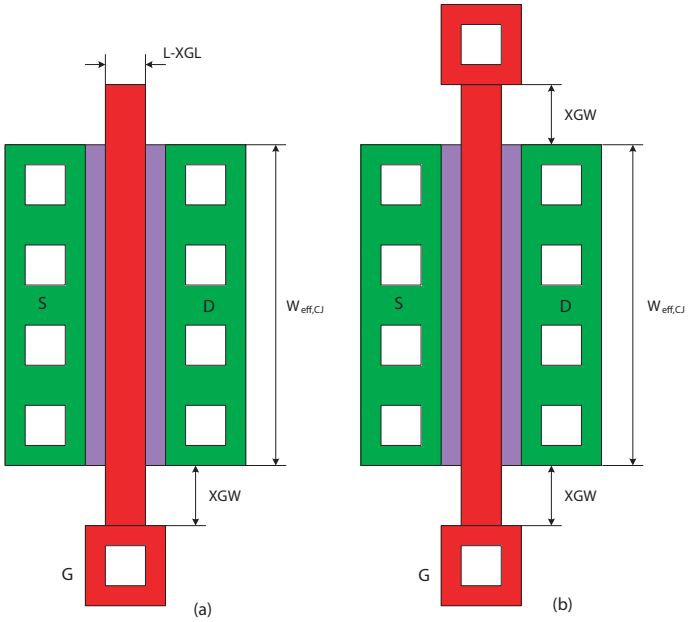


Figure 3.3: Geometrical details for calculating the gate resistance (a)$NGCON$=1, (b)$NGCON$=2.

the gate contact and the channel edge, and XGL is the difference between the L specified in the MOSFET instance statement and the physical gate length.

If we assume that the gate is contacted at one side $NGCON$=1 (Figure 3.3a), XGW=XGL=0 and NF=1 the equation (3.6) simplifies to:

$$R_{Geltd} = \frac{1}{3} RSHG \frac{W_{eff,CJ}}{L}. \tag{3.7}$$

The factor *1/3* accounts for the distributed nature of the current conduction as derived in [Liu 98]. The case when the gate is contacted form both sides ($NGCON$=2) is illustrated in Figure 3.3b. If XGW=XGL=0 and NF=1 then the equation (3.6) becomes

$$R_{Geltd} = \frac{1}{12} RSHG \frac{W_{eff,CJ}}{L}. \tag{3.8}$$

As $NGCON$ increases from 1 to 2, one might expect the factor to halve form *1/3* to *1/6*. The reason that the resistance decreases by four-fold is because the location at which the gate current equals zero occurs at x=$W_{eff,CJ}/2$, rather than $W_{eff,CJ}$. The resistance already decreases by two-fold because of the width reduction, and the overall resistance decreases by another two-fold due to the presence of two gate contacts in parallel.

When $RGATEMOD$=2, BSIM4 model uses a "channel-reflected gate resistance" ($R_{G,crg}$) in addition to gate resistance $R_{G,eltd}$. $R_{G,crg}$ represents the first order non-quasi-static effects in the channel, since it is not a physical resistance it does not

include a thermal noise source. This gate source resistance component is critical in matching the noise data and is defined as

$$R_{G,crg} = \frac{1}{XRCRG1\left(\frac{I_{ds}}{V_{dseff}} + XRCRG2\frac{kT}{q}\mu_{eff}\frac{W_{eff}}{L_{eff}}C'_{ox,IV}NF\right)} \tag{3.9}$$

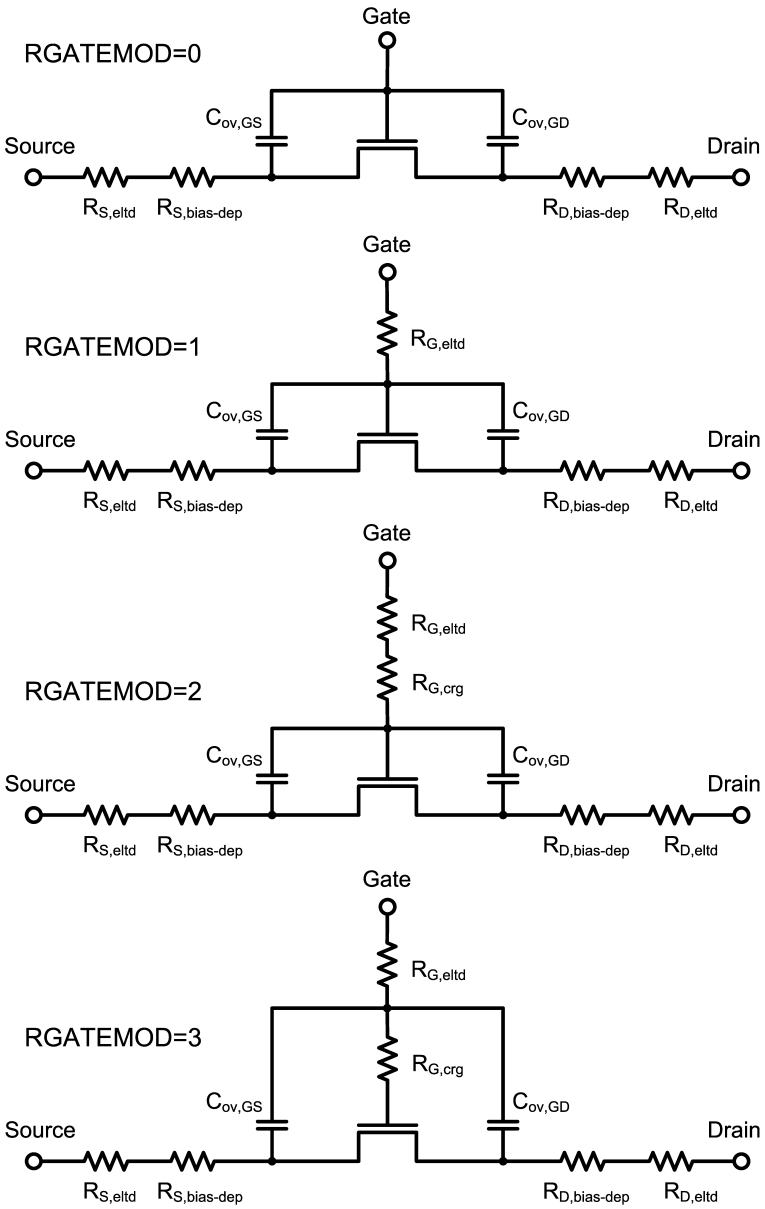


Figure 3.4: Gate resistance modeling at different *RGATEMOD* settings.

When the selector *RGATEMOD*=3 the location of the overlap capacitances is different. The equivalent circuits for all *RGATEMOD* settings are illustrated in Figure 3.4.

Noise modeling

The following noise sources are modeled in BSIM4:

- flicker noise
- channel thermal noise
- induced gate noise and the correlation with channel thermal noise
- shot noise due to the gate tunneling current
- thermal noise due to the resistances at the terminals

Different model selectors have been introduced to use the noise models in the simulations.

Flicker Noise Models

BSIM4 includes two different flicker noise models. The *fnoiMod* selector is introduced to define the model in the simulation. If *fnoiMod*=0, a simple flicker noise model is used. The drain current noise is defined as:

$$\overline{i_d^2}|_{Flicker} = \frac{KF(I_{ds})^{AF}}{C'_{ox,IV}L_{eff}^2 f^{EF}}\Delta f. \tag{3.10}$$

If *fnoiMod*=1, a unified flicker noise model is used. This is an improved BSIM3v3 model, where the noise characteristics predicted by the model transit smoothly over different bias regions and the bulk charge effect has been accounted for. This is a default model used in the simulation. The drain current noise is defined as [Liu 01]:

$$\overline{i_d^2}|_{Flicker} \approx f'(NOIA, NOIB, NOIC)\left[\frac{I_{ds}}{C'_{ox,IV}L_{eff}^2 f^{EF}} + \frac{g'(EM)I_{ds}}{W_{eff}L_{eff}^2 f^{EF}}\right]\Delta f \tag{3.11}$$

Channel Thermal Noise Models

BSIM4 provides two options for the channel thermal noise. The selector *TNOIMOD* is used to choose between the charge-based model and holistic thermal model. The charge-based model (*TNOIMOD*=0) defines the channel thermal noise as

$$\overline{i_d^2} = \frac{4kT\cdot NTNOI}{R_{DS} + L_{eff}^2/(\mu_{eff}|Q_{inv}|)}\Delta f \tag{3.12}$$

If *TNOIMOD*=1 the holistic thermal model is used. In this model, all the short-channel effects including the velocity saturation effect incorporated in the I-V model are automatically included in the noise calculation. Additionally the modeling captures the amplification of the channel thermal noise through g_m and g_{mb}

as well as the induced gate noise with the correlation to the channel thermal noise. The noise source in the holistic model is given by

$$\frac{\overline{i_d^2}}{\Delta f} = 4kT\frac{V_{dseff}}{I_{ds}}\left(\beta g_m + \beta g_{mb} + g_d\right)^2 - 4kTR_x\left(g_m + g_{mb} + g_d\right)^2, \tag{3.13}$$

where

$$R_x = \theta^2\frac{V_{dseff}}{I_{ds}}, \tag{3.14}$$

$$\beta = 0.577 \times \left[1 + TNOIA\cdot L_{eff}\left(\frac{\mu_{eff}V_{gseff}}{2VSAT\cdot L_{eff}}\right)^2\right], \tag{3.15}$$

$$\theta = 0.37\left[1 + TNOIB\cdot L_{eff}\left(\frac{\mu_{eff}V_{gseff}}{2VSAT\cdot L_{eff}}\right)^2\right]. \tag{3.16}$$

Shot noise model due to the gate tunneling current

The modeling of the shot noise contributed from the gate tunneling current is also provided in BSIM4. The shot noise spectral density is given by [Ytterdal 03]:

$$\frac{\overline{i_{gtx}^2}}{\Delta f} = 2qI_{gtx}, \tag{3.17}$$

where I_{gtx} can be one of the following tunneling currents: the gate-to-source tunneling current, the gate-to-drain tunneling current, or gate-to-substrate tunneling current.

Thermal noise models for parasitic resistances

BSIM4 includes the thermal noise contribution from parasitic resistances at the gate, the drain, the source and the substrate. The power spectral densities of the thermal noise currents for the following resistances are given by:

- gate resistance
$$\frac{\overline{i_{R_G}^2}}{\Delta f} = \frac{4kT}{R_G}, \tag{3.18}$$
- drain resistance
$$\frac{\overline{i_{R_D}^2}}{\Delta f} = \frac{4kT}{R_D}, \tag{3.19}$$
- source resistance
$$\frac{\overline{i_{R_S}^2}}{\Delta f} = \frac{4kT}{R_S}, \tag{3.20}$$
- substrate resistance
$$\frac{\overline{i_{R_{subx}}^2}}{\Delta f} = \frac{4kT}{R_{subx}}, \tag{3.21}$$

where R_{subx} can be R_{BPS}, R_{BPD}, R_{BSB}, R_{BDB} or R_{BPB}.

Table 3.1: Parameter explanations

Parameter	Description
A_{bulk}	Bulk-Charge coefficient
$ALPHA0$	First parameter of the substrate current due to impact ionization
$ALPHA1$	Modified first parameter to account for length variation in the calculation of I_{sub}
$BETA0$	Second parameter of the substrate current due to impact ionization
C_{CLM}	Channel length modulation coefficient
$C'_{ox,IV}$	Effective oxide capacitance for I-V calculation
EF	Flicker noise frequency exponent
EM	Saturation field
KF	Flicker noise coefficient
L_{eff}	Effective channel length
NF	Number of transistor fingers
NGCON	Number of gate contacts per finger
NOIA	First Flicker noise parameter
NOIB	Second Flicker noise parameter
NOIC	Third Flicker noise parameter
NTNOI	Model parameter for simulation accuracy improvement
Q_{inv}	Total inversion layer charge
R_{DS}	Source/drain resistance
RSHG	Gate electrode sheet resistance
V_{ACLM}	Early voltage for the CLM effect
V_{ADIBL}	Early voltage for the DIBL effect
V_{ADITS}	Early voltage at the DITS effect
V_{ASAT}	Early voltage at the saturation voltage point
V_{ds}	Drain to source voltage
VSAT	Saturation velocity
V_{dseff}	Effective drain to source voltage
V_{gsteff}	Effective $V_{GS} - V_T$ smoothing function
W_{eff}	Effective channel width
$W_{eff,CJ}$	Effective with of the junction capacitance calculation
XGL	Difference between L and the physical length
XRCRG1	First parameter of channel-reflected gate resistance
XRCRG2	Second parameter of channel-reflected gate resistance
XGW	Distance from the gate contact to the channel edge
μ_{eff}	Effective mobility

3.1.2 MOS Varactors

MOS varactors are capacitors with voltage controlled capacitance. They are commonly used circuits requiring tunable LC-resonators.

A cross section of a NMOS varactor on a p^- substrate and a small-signal equivalent circuit formed by a series connection of a variable capacitance and a variable resistance are illustrated in Figure 3.5.

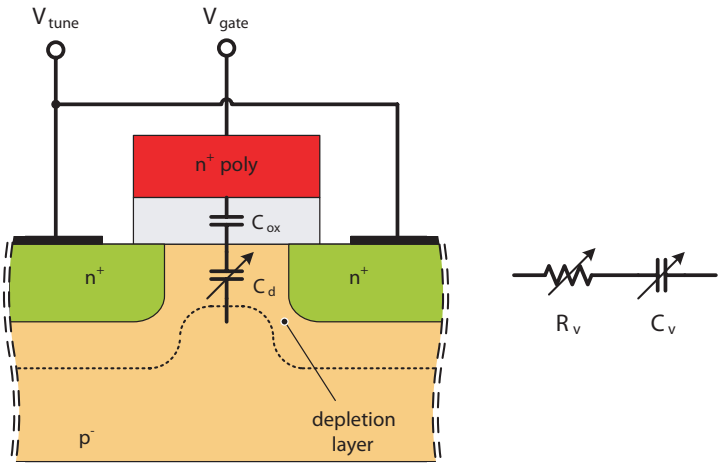


Figure 3.5: Cross section of a NMOS varactor in depletion mode and a small-signal equivalent model.

The MOS varactor can be formed from a MOS transistor in which the drain and the source are shorted. This forms a three-terminal device with the gate, the drain-source and the bulk contacts. The bulk terminal is grounded, the capacitance tuning voltage V_{tune} is applied to the source-drain terminal and the voltage V_{gate} is applied to the gate terminal.

The variable capacitance C_v is formed by a series connection of the gate oxide capacitance C_{ox} and the depletion region capacitance:

$$\frac{1}{C_v} = \frac{1}{C_{ox}} + \frac{1}{C_d} \tag{3.22}$$

The device can operate in three modes depending on the voltage V_{gate}. Figure 3.6 shows the NMOS varactor in all three modes with the relevant lumped components and the small-signal capacitance at zero tuning voltage. The NMOS varactor operation is either in the accumulation mode, the depletion or the inversion mode [Maget 02]. The device is in accumulation as the negative voltage is applied to the gate resulting in the excess of holes at the surface of the semiconductor. The varactor capacitance has the maximum value determined by the gate oxide capacitance C_{ox}. In the accumulation mode the series resistance R_v is formed by

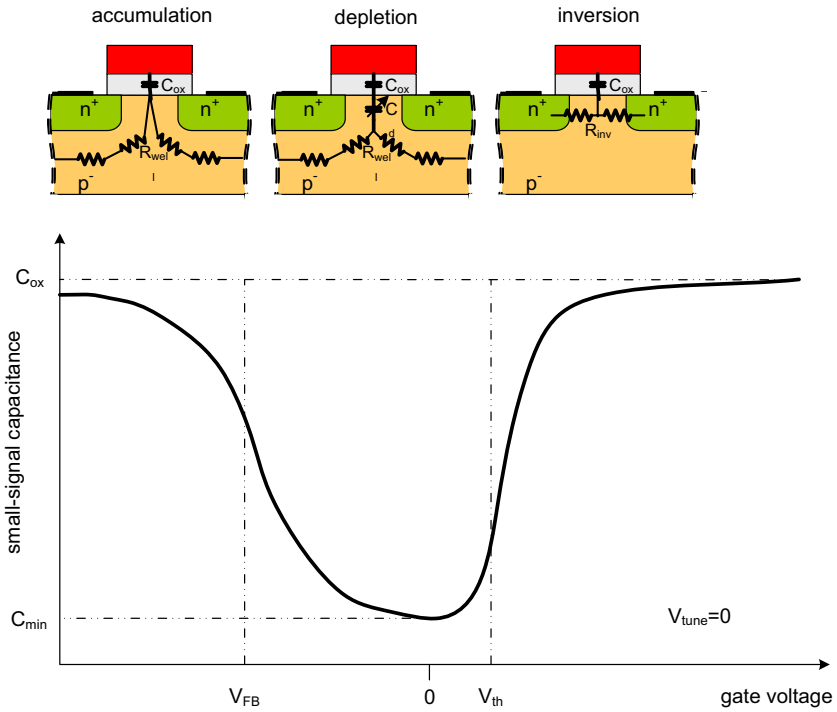


Figure 3.6: Typical small-signal voltage-capacitance characteristic of an NMOS varactor with corresponding lumped elements at zero tunning voltage.

the gate resistance in series with the resistance from the accumulation layer to the substrate (well) contacts outside the device.
As the gate voltage increases the flat-band situation is reached. The semiconductor beneath the gate is neutral and the gate charge is balanced by fixed oxide and interface charges. The flat-band voltage V_{FB} is usually negative and if the gate and well have the same doping type occurs close to zero.
When the gate voltage excesses the V_{FB} voltage holes are repelled from the surface and the negatively charged ions of fixed acceptors are repelled from the depletion region. The gate charge is balanced by more or less negative dopands, i.e. by a wider or shallower depletion region. The capacitance is essentially that of the gate oxide C_{ox} in series with the variable depletion region capacitance C_d. The resistance R_v is lower than in the accumulation, as the resistive path is shorter.
The device enters the inversion as the gate voltage exceeds a certain threshold voltage V_{th}. In this situation the depth of the depletion region remains constant and the electron inversion layer balances the changes in the gate charge. The varactor capacitance is determined only by the gate oxide capacitance C_{ox}. The resistance R_v is determined by the inversion layer. When the semiconductor surface is weakly inverted with few electrons a peak of resistance is observed. The resistance drops to low value as the strong inversion is reached (high gate voltage) and it is proportional to the gate length of the varactor.

3.1.3 C11 RF2 substrate

C11 RF technology features 4 copper thin metalization layers and two thick aluminum top metal layers. The cross section of the substrate is shown in Figure 3.7. The dielectric filling the space between the metals is silicon oxide with ϵ_r=4.1. The top metal is covered with a layer of polyimide except form the pad openings.

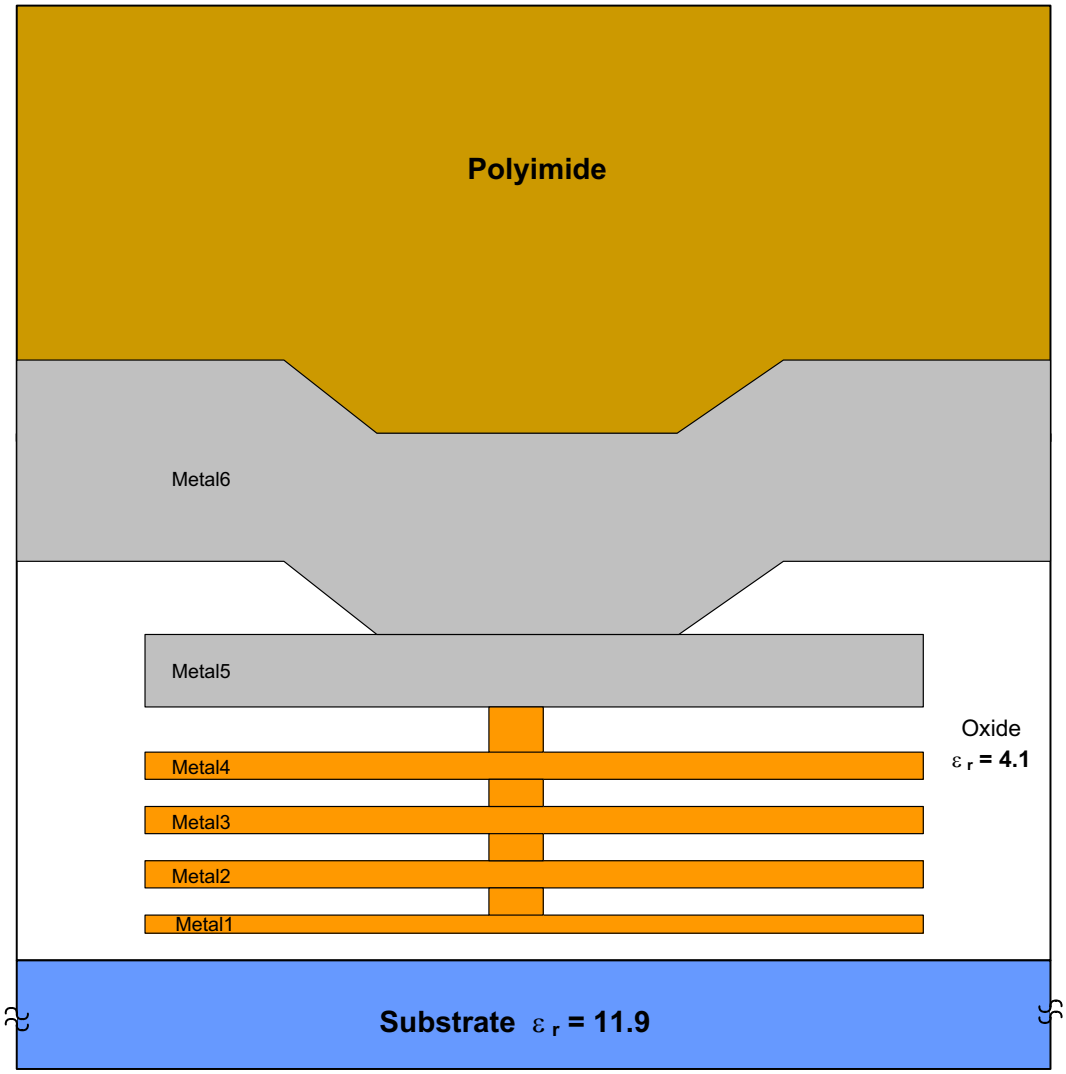


Figure 3.7: A simplified cross section of C11 RF substrate showing available metalization layers.

3.1.4 Inductors

Inductors are commonly used in RF circuits in matching networks or resonant load tanks. They can be realized as planar multi-layer structures. Within this work symmetrical inductors where desired as all receiver blocks employing them have differential structure. Symmetrical structures are preferred for their inherent low sensitivity to substrate noise. However, the layouts and modeling are more complicated for such inductors. A 3D view of a symmetrical inductor is shown in Figure 3.8.

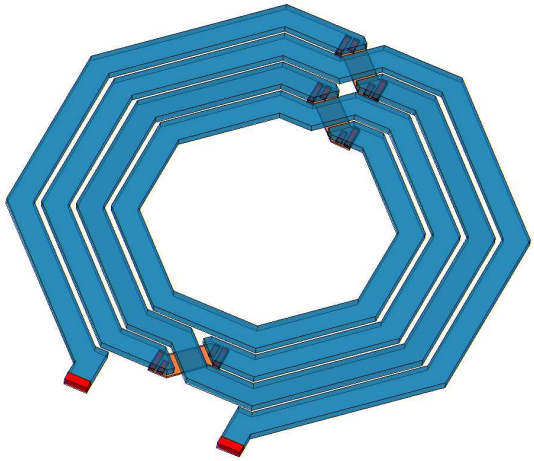


Figure 3.8: 3D view of a cross-coupled symmetrical inductor.

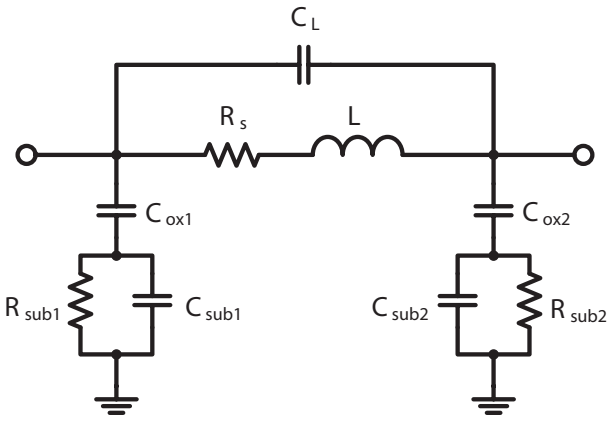


Figure 3.9: Lumped component model of an inductor.

A physical lumped-component π-model representing the electronic behavior of a spiral inductor is shown in Figure 3.9. The model parameters are described as:

- L: The total inductance caused by the magnetic flux density $\overrightarrow{B}$ of the electromagnetic field.
- R_S: The series resistance of the metal traces with finite conductivity, skin effect and crowding current.
- R_{sub}: The resistance modeling the losses in the substrate.
- C_L: The capacitance modeling the lateral coupling between the turns of the inductor.
- C_{ox}: Models the oxide capacitance above the substrate.
- C_{sub}: Models equivalent substrate capacitance.

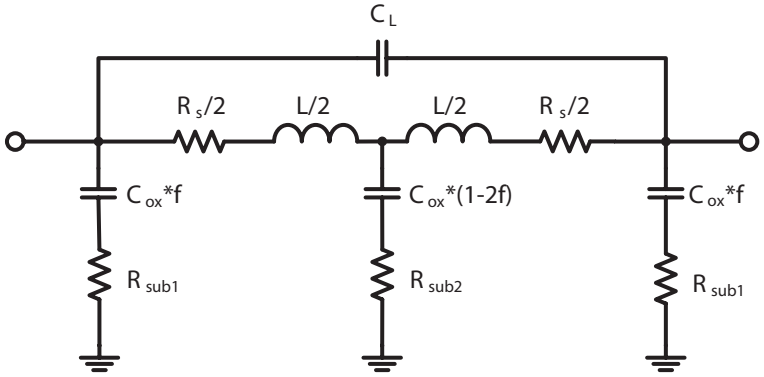


Figure 3.10: Symmetrical inductor equivalent circuit.

In case of symmetrical inductors the π-model must be extended as shown in Figure 3.10. This model allows accurate modeling of the coil in a balanced and in a single-ended configuration. Additionally to single-ended model parameters a f factor is introduced to distribute the overall parasitic capacitance to each branch. The lumped component modeling does not give accurate inductor characterization either at high frequencies nor in large bandwidth. To fulfill those requirements numerical methods implemented in electromagnetic simulators have to be employed. The most commonly used field solver methods are:

- *method of moments(MoM)* implemented in Agilent MOMENTUM [Momentum 07] and best suited for planar structures
- *finite element method (FEM)* used in HFSS [HFSS 07] and dedicated for 3D structures.

3.1.5 Capacitors

Capacitors are essential components in this work. They are used in matching networks, as AC coupling components and as decoupling (blocking) components on DC lines. In RF applications the capacitors should feature self resonance frequencies well in excess of the frequency of operation and high quality factors Q, as well as good linearity and large break-down voltages. The capacitance density and the ratio between the desired capacitance and parasitic capacitance $C/C_{parasitic}$ fulfill the list of key parameters characterizing integrated capacitors. C11 RF technology provides several capacitor types with different characteristics.

MOS capacitors

MOS capacitors use the capacitance between the gate and connected source and drain contacts. The structure is similar to the varactor structure presented in Figure 3.5. The capacitors are not linear, require biasing, suffer from a relatively high series resistance and have low break-down voltage. However, a MOS capacitor features high capacitance density ($\approx 11\,\mathrm{fF}/\mu m^2$) and therefore being attractive for structures requiring high capacitance values as for instance blocking capacitors on DC lines.

Metal-Oxide-Metal and Metal-Insulator-Metal capacitors

The capacitors used for AC coupling in the signal path are required to be linear and have high quality factor. Such capacitors are commonly realized as parallel plate structures using the metalization layers [Aparicio 02]. A Metal-Oxide-Metal

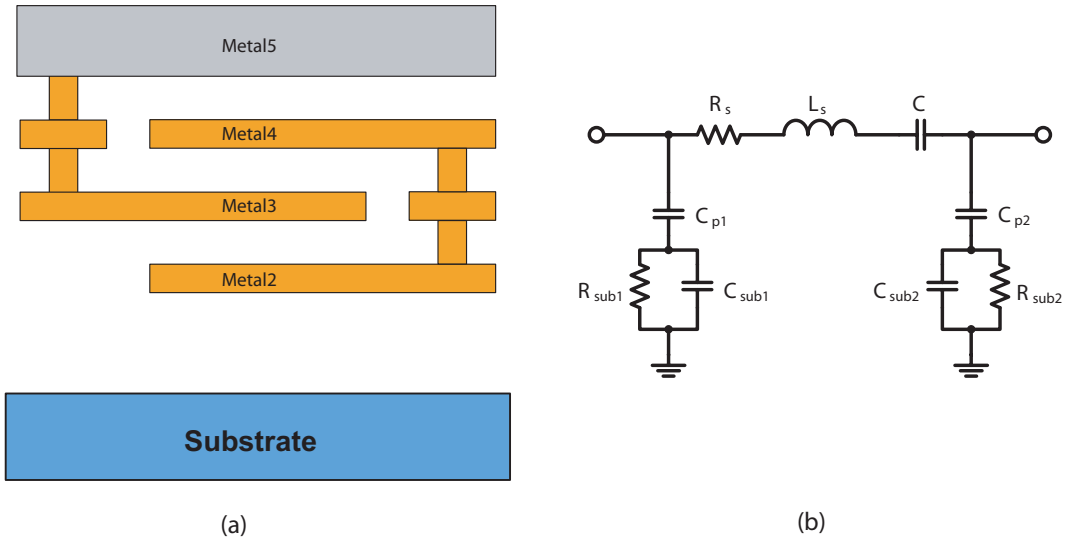


Figure 3.11: a) Cross section of a Metal-Oxide-Metal capacitor, b) equivalent circuit.

(MOM) parallel plate capacitor and its equivalent circuit are shown in Figure 3.11. The overall capacitance is determined by a parallel connection of three capacitors

formed by four metal plates. The MOM capacitors suffer from a low capacitance density which mainly arises from the large metal-to-metal spacing. The parasitic capacitance to the substrate is significant and introduces losses at signal coupling. A Metal-Insulator-Metal (MIM) capacitor features high quality factor, low dielectric loss and high capacitance density. It has a parallel plate structure using an extra dielectric layer with reduced thickness. The MIM capacitors in C11 RF technology are realized in top metalization layers. Due to this fact the parasitic capacitance to the substrate is minimized. The cross section and the equivalent circuit of a MIM capacitor are shown in Figure 3.12.

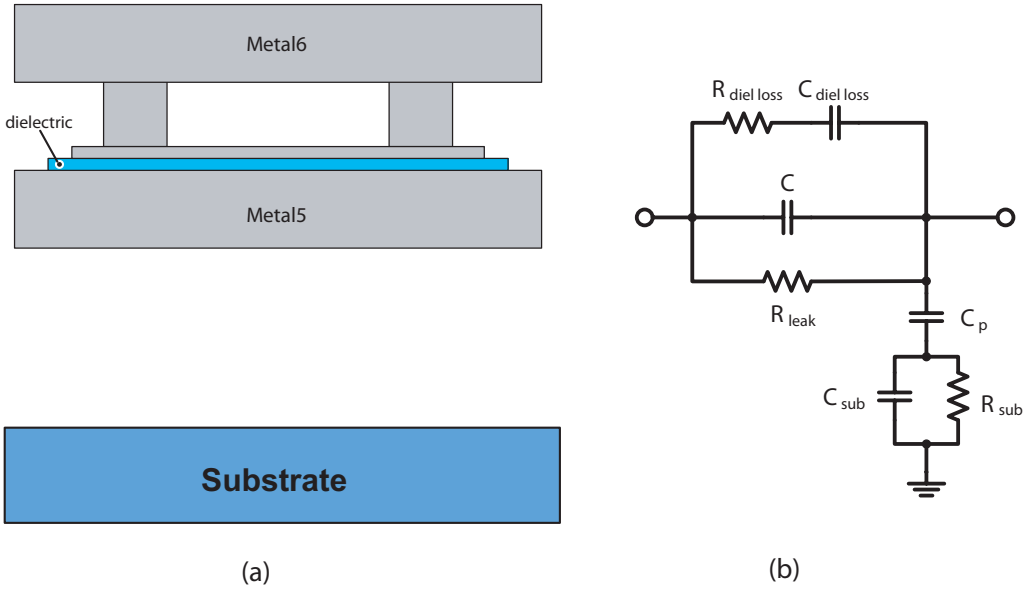


Figure 3.12: a) Cross section of a Metal-Insulator-Metal capacitor, b) equivalent circuit.

Chapter 4

Multi-Band Adaptive Receiver Architecture and Specifications

4.1 Introduction

Nowadays users require the same quality and service from a wireless network as offered by wired networks. Email, Internet access, video distribution, access to peripheral devices, and replacement of Ethernet network installations are example applications over wireless links. However, popular second- (2G) and third-generation (3G) technologies do not fulfill those requirements. Even wireless short-range wireless communication networks seem to be one generation behind their wired counterparts, limiting their use as convenient replacement technology. Therefore, the Wireless Gigabit with Advanced Multimedia (WIGWAM) project was established to develop a wireless short-range transmission technology capable of competing with wired LANs. The project aims to develop wireless short-range communication system offering adaptive data rates up to maximum of 1 Gb/s using carrier frequencies in 5, 17, 24, and 60 GHz bands. OFDM (orthogonal frequency division multiplexing) is chosen as modulation format. To support IEEE 802.11g/n devices in the same frequency range, bandwidth is kept flexible in n x 20 MHz steps, up to 100 MHz [Fettweis 05], [Eberts 05].
Within this work the development and implementation of a multi-band and multi-standard adaptive receiver operating in 5 GHz and 24 GHz bands is carried out. A system concept of an adaptive receiver with analog preprocessing is proposed and the circuit implementation in a cost effective CMOS technology is performed.

4.2 System Concept

The development of a hardware platform capable of reception and processing data rates at 1 Gb/s requires the definition of key requirements which are:

- multi-band operation - support 5 and 24 GHz frequency ranges
- multi-mode operation - compatibility with existing wireless standards in the same frequency ranges (IEEE 802.11a/n)
- time-average current consumption control - to support MIMO operation
- the choice of technology ensuring long-term competitiveness

A long term competitiveness of new wireless products can be ensured by a cost-effective CMOS technology. However, to fulfill the WIGWAM project requirements also components operating in frequency ranges up to 60 GHz have to be designed which for the time being can be realized in BiCMOS technology. Since there is no possibility to use same technology for all the components of a multi-band receiver, a hybrid architecture consisting of a 5 GHz base platform and 17/24/60 GHz down-converters is proposed. The goal of this work was to develop a receiver operating at 5 GHz and 24 GHz bands and therefore the further discussion will be limited only to those bands.

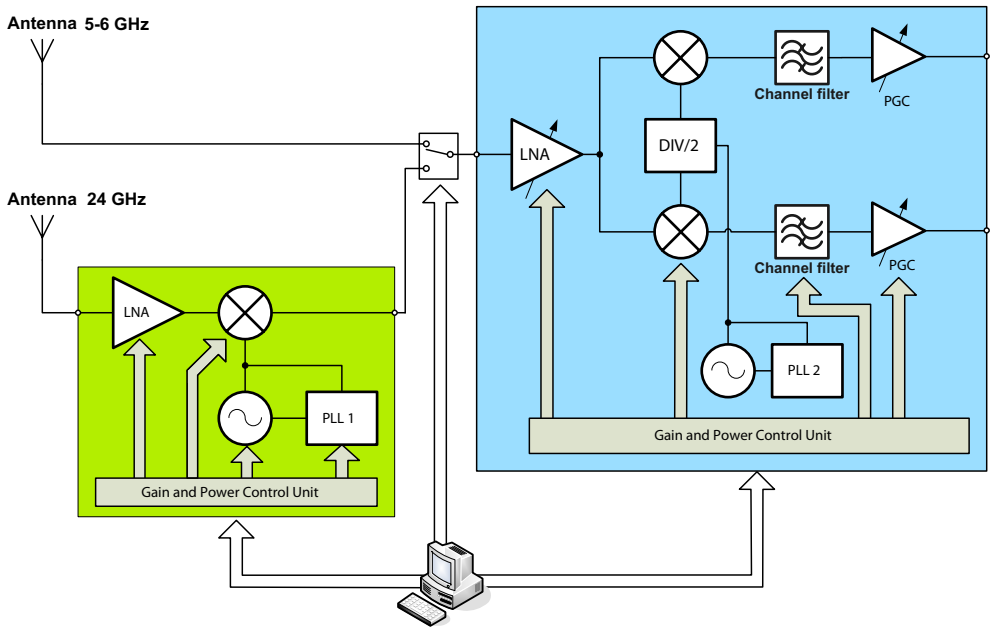


Figure 4.1: Block diagram of the proposed hybrid receiver.

A homodyne architecture is chosen for the 5 GHz receiver supporting IEEE 802.11a, IEEE 802.11n and WIGWAM standards. For 24 GHz band a heterodyne architecture consisting of a down-converter in front of the 5 GHz part will be used, as shown in Figure 4.1. Such arrangement allows multiple usage of most functional blocks and thus considerably reduces the frequency synthesis complexity. The concept of the 5 GHz receiver working in the hybrid mode allows to support new standards occupying additional frequency bands such as e.g. IEEE 802.16 (WiMAX).
In order to obtain required high spectral efficiency, MIMO operation in parallel signal processing in analog part is required. However, parallel operation of e.g. four receiver paths with conventional circuitry increases the current consumption by several times and becomes not feasible in battery-powered applications. This problem cannot be solved by usage of smaller structures like in case of digital applications, since the main parameters of an analog RF front-end like noise figure and linearity strongly depend on the consumed current. Moreover, for future multi-standard receivers e.g. software defined radio, handling different signal dynamic ranges with the same hardware will be essential for cost and complexity of the hardware. Additionally, the analysis of ISM band showed that only in rare cases the receiver system operates at the sensitivity limit defined by the system specification and with simultaneous presence of an interferer at the upper limit [Biggs 04]. So far receivers were designed to meet such extreme requirements constantly leading to current consumption significantly higher than actually required. Therefore, a receiver with an adaptation of operating points (e.g. currents) with respect to the respective interferer power present at the receiver input can feature significantly reduced time-average power consumption.

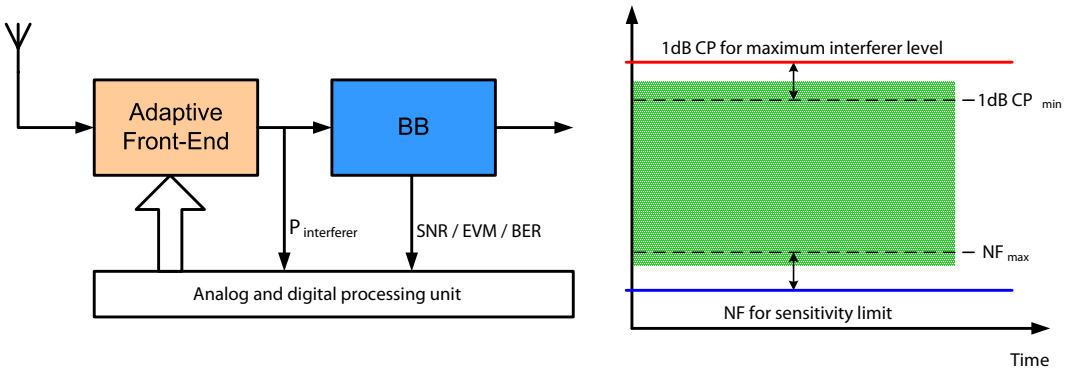


Figure 4.2: Adaptive front-end with the sensitivity and the linearity adaptation.

Such an adaptation technique can be implemented either with a combination of analog and digital processing or pure analog pre-processing. The adaptation technique employing analog and digital processing is shown in Figure 4.2. It adopts the sensitivity limit and the large signal capability of the receiver according to

the actual received signal. Such technique enables many possibilities for efficient power consumption but features an additional delay in the adaptation due to the usage of digital signal processing for SNR (or BER, EVM) calculation.
The pure analog pre-processing technique adopts only the large signal capability to the actual received signal as shown in Figure 4.3. By appropriate circuit concepts and adaptation of gain/noise figure constellation in the signal chain is provided and the sensitivity limit always stays within system specification.

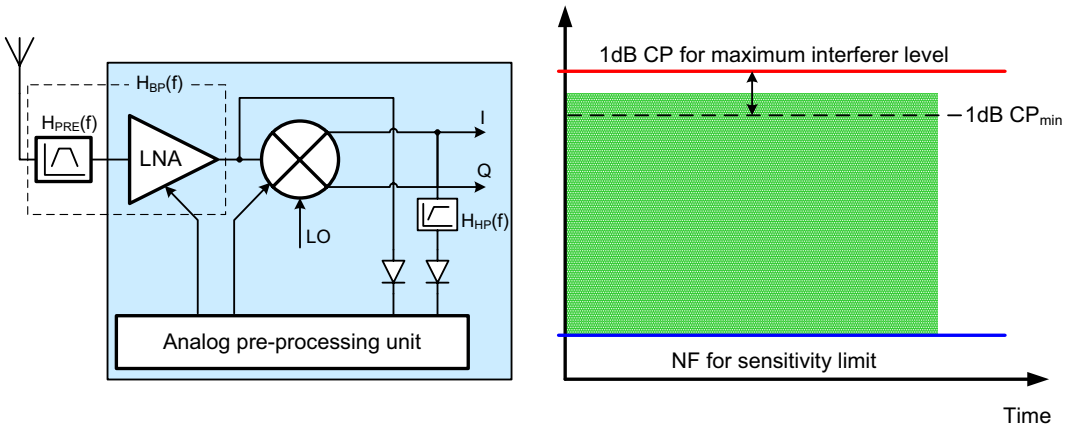


Figure 4.3: Adaptive front-end with analog pre-processing for the linearity adaptation.

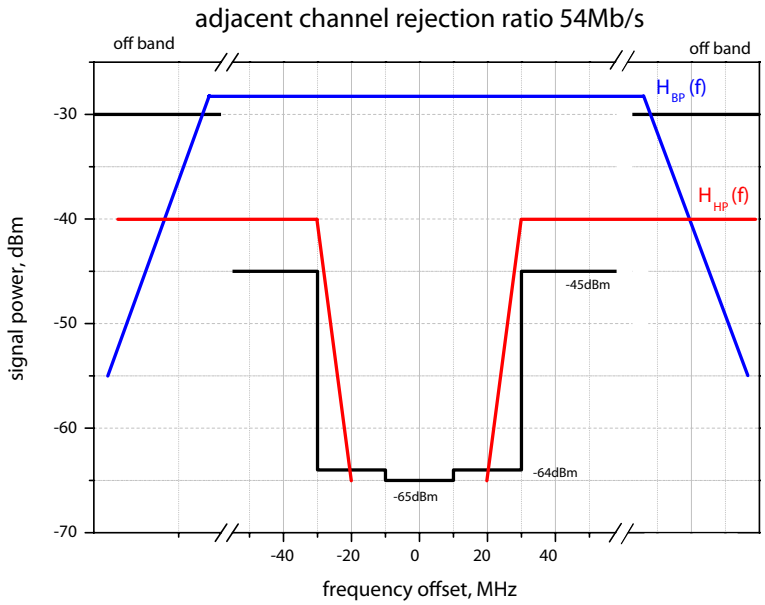


Figure 4.4: Filtering method for interferer power measurement.

In this technique the actual interferer (blocker) power is calculated and then the gain and current settings required to maintain the given desensitisation limit are deducted. The interferer power is determined by the overlapping of two filter transfer functions. Such measurement method yields the actual integral interferer power present in the whole band. Figure 4.4 shows the measuring procedure of the power of all relevant interferers. The useful band is selected by a pre-filter with transfer function $H_{PRE}(f)$, placed after the antenna and the narrow-band transfer function of the LNA $H_{LNA}(f)$ yielding in the input bandpass characteristic

$$H_{BP}(f) = H_{PRE}(f) \cdot H_{LNA}(f) \tag{4.1}$$

In oder to characterize the power in adjacent channels the second filter with high-pass transfer function ($H_{HP}(f)$) is employed.The power detectors should feature a flat (wide band) frequency response over the whole frequency band e.g over several octaves of the received signal transformed into the baseband domain.

4.2.1 Link Budget Parameters

The system requirements for Home/Office scenario where calculated by the project partner. The required sensitivity for 5 GHz frequency range is -60 dBm for the noise bandwidth of 96.25 MHz and SNR_{min} of 25 dB. Those parameters set up the limit on the noise performance of the receiver which can be calculated from the formula defining the system sensitivity given as

$$S_{min} = -174\,dBm/Hz + NF + 10\log\,B + SNR_{min}. \tag{4.2}$$

Rearranging the above formula for noise figure yields:

$$NF = S_{min} + 174\,dBm/Hz - 10\log\,B - SNR_{min}. \tag{4.3}$$

Finally the required noise figure of the receiver can be calculated:

$$NF = -60\,dBm + 174\,dBm/Hz - 10\log\,(96.25\,MHz) - 25\,dB\;=\;9.17\,dB \tag{4.4}$$

The calculated noise figure includes the loss introduced by an off-chip band-select filter which is assumed to be 4 dB. The required noise figure for the receiver has to be then corrected for this value and finally setting the receiver noise figure to be less than 5 dB.
The ADC input level of -8 dBm should be achieved. Knowing the required sensitivity and the output level the overall receiver gain can be calculated as

$$Gain_{RX} = P_{ADC} - (S_{min} - 4\,dB) = -8\,dB - (-60\,dB - 4\,dB) = 56\,dB, \tag{4.5}$$

where 4 dB denotes the loss of the band-select filter. The link budget parameters for the 5 GHz receiver are summarized in Table 4.1.
The 24 GHz down-converter should operate in an unlicensed band at 24-24.25 GHz

but there is no standard available. The goal of the project is to prove that key receiver components implemented in a CMOS technology can provide comparable results to other expensive solutions. Therefore, a conversion gain of more than 20 dB and a noise figure of less than 7 dB where chosen as the limiting parameters for a 24 GHz down-converter.

Table 4.1: Link budget parameters for a 5 GHz receiver.

Parameter	Symbol	Value	Unit
Frequency	F	5	GHz
Noise Bandwidth	B	96.25	MHz
Signal-to-Noise Ratio	SNR_{min}	25	dB
Sensitivity	S_{min}	-60	dBm
Receiver Noise Figure	NF_{RX}	≤ 5	dB
Receiver Gain	$Gain_{RX}$	56	dB

4.2.2 Level Plan and Circuit Specification

Having defined the required overall noise figure and gain of the receiver the specifications of the receiver components have to be defined. The gain of the receiver is partitioned in the way that 30 dB is assigned to the LNA and the mixer and the rest of 26 dB should be achieved by the analog baseband consisting of a Programmable Gain Amplifier (PGA) and a Base-Band (BB) filter. At very high input signals, when the SNR is above 25 dB, the gain of the LNA and the mixer should be reduced to 20 dB.

Low Noise Amplifier

As the first stage of the receiver the LNA should provide sufficient gain to amplify the signals sufficiently above the noise floor, while having minimized noise contribution. The gain value has to be balanced taking into consideration the linearity capability of the following stages. Additionally, the LNA should provide good input match to 50 Ω impedance of an external filter or an antenna. It should be able also to cope with the highest allowable signals appearing at the antenna, which sets the linearity requirements. Taking all the requirements into consideration the gain of 20 dB and the noise figure of 2.5 dB where chosen as the target values.

Mixer

The mixer is required to deliver the gain of 10 dB with the maximum noise figure of 15 dB. Those values guarantee acceptable noise contribution to the overall performance of the receiver. The highest signal level sets up the linearity requirement and the 1 dB ICP of -15 dBm was chosen as the target value.

Analog Base-Band

The BB part should achieve the gain of 26 dB and realize the filtering with tunable cut-off frequency for multi-standard operation. A constant output level signal of -8 dBm required an application of a PGA. In order to reduce the linearity requirements for the BB analog part two PGAs will be used, one in front of the filter and the other at the end of the receiver chain. Such configuration relaxes the noise requirements of the filter as well. The PGA should feature a tunable gain between 0 dB and 14 dB and a 1 dB ICP of -14 dBm. The filter should achieve the cut-off frequencies of 10,20, and 50MHz , and finally an attenuation of 3 dB and a 1 dB ICP of -14 dBm are assumed.

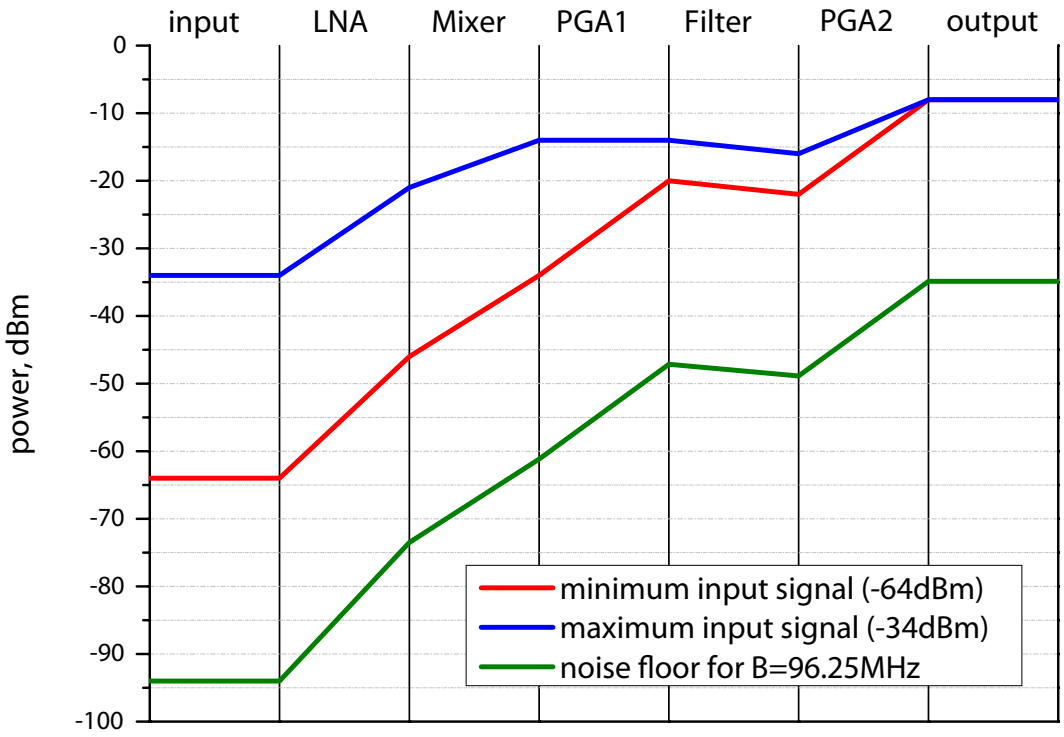


Figure 4.5: Level plan of the 5 GHz receiver.

Table 4.2 summarizes the specifications of the receiver building blocks. Finally Figure 4.5 shows the level diagram of the proposed receiver architecture.

Table 4.2: Summary of the derived specifications for the receiver building blocks.

LNA	Input Reflection Coefficient (S_{11})	$<$ -10 dB
	Noise Figure (NF)	$<$ 2.5 dB
	Gain	20 dB
Mixer	Conversion Gain	10 dB
	Noise Figure (NF)	$<$ 15 dB
	1 dB Input Compression Point	$>$ -15dBm
PGA	Gain	0$\div$14 dB
	Noise Figure (NF)	$<$ 15 dB
	1 dB Input Compression Point	$>$ -15dBm
Base-Band Filter	Cut-off Frequency	10,20,50 MHz
	Noise Figure (NF)	$<$ 30 dB
	Gain	-3 dB
	1 dB Input Compression Point	$>$ -15dBm

Chapter 5

Multi-Band Adaptive Receiver Implementation

5.1 5-6 GHz Zero-IF Receiver with Analog Pre-Processing

The block diagram of the implemented 5 GHz homodyne receiver is shown in Figure 5.1. The receiver path consists of a differential LNA, followed by quadrature mixers. After the I/Q-mixers the signal is fed into a channel-select filter surrounded by two PGAs. The output base-band signal is then buffered with an amplifier in order to drive 50 Ω termination impedance. The LO signal for quadrature demodulator is delivered from a VCO followed by a 1:2 divider. The analog pre-processing circuit consists of a power detector, a comparator and an inverter. The power detector measures the down-converted signal power and the measurement result is compared with a reference voltage. According to the comparison result the gain of the PGAs proceeding and following the BB filter is adjusted.
The channel selection filter is a 5^{th} order Sallem-Key structure. The filter supplies no gain while rising the overall noise figure significantly. In order to suppress the noise contribution of the filter two PGAs were used, one in front of the filter one after the filter. The first PGA works when the receiver has to deal with the useful signals of low power. The second amplifier is used when strong interferer signals are received and the linearity of the receiver is therefore the issue. Such configuration significantly reduces the noise contribution of the filter while providing constant gain of the receiver chain.
The power consumption of each of the receiver blocks is digitally controllable by means of a set of tunable current sources. Additionally to the power consumption a digital controlling of the gain and frequency of operation is implemented. In order to externally program all the control bits a serial interface is used. It consists of an address decoder and shift registers. A Windows application is used to setup control bits and load the data to the receiver over LPT port.

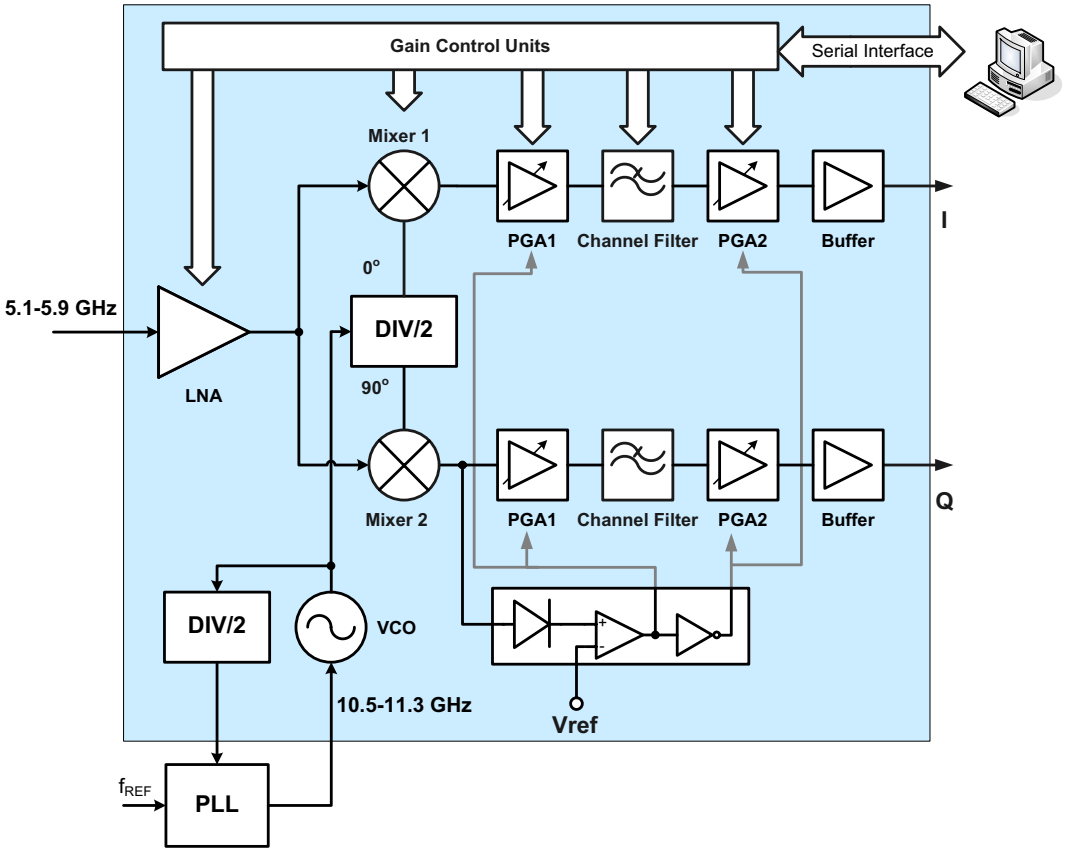


Figure 5.1: Block diagram of the integrated receiver.

5.2 Low Noise Amplifier

The LNA as the first component in the receiver chain sets the limits on the overall sensitivity. Therefore, low noise is one of the most important design goals. The input stage should also feature sufficient gain to suppress the noise of the following stages and good linearity to handle out-of-band interferers. Furthermore, the LNA should provide well defined input impedance, which is normally 50 Ω, to match to an antenna or an external band-select filter. Finally for product-oriented applications the electrostatic discharge (ESD) robustness is required as the LNA is connected to the outer world through an antenna. Taking into account all the requirements, a careful analysis and comparison of various gain stages must be carried out to chose the right topology for this crucial component.

5.2.1 Common-Source and Common-Gate LNA

Common-Source LNA with inductive degeneration

The common-source amplifier with inductive degeneration has been commonly used showing good performance [Shaeffer 97], [Chang 05], [Li 06]. The amplifier employs two inductors to provide input matching and resonant LC-tank as the load, as shown in Figure 5.2.

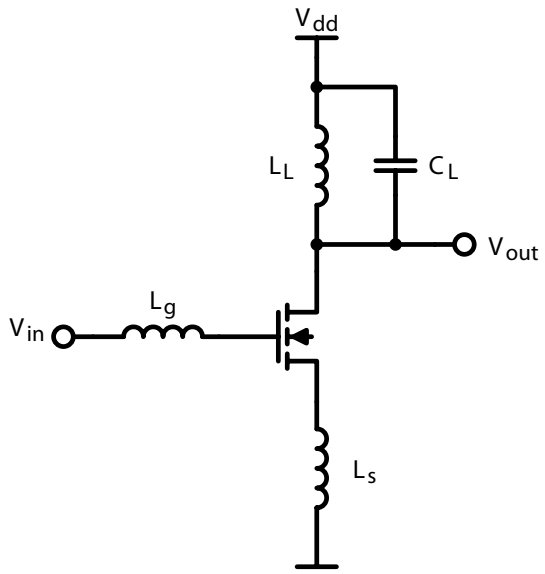


Figure 5.2: Common-source amplifier with inductive degeneration.

A simple analysis of the input impedance shows that

$$Z_{in} = s\,(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}} L_s \tag{5.1}$$

The source inductance L_s introduces a real part in the input impedance which has to be matched to the source impedance R_s so that

$$R_s = \frac{g_m}{C_{gs}} L_s = \omega_T L_s \tag{5.2}$$

Once the inductance L_s is chosen to adjust the real part of the impedance, the gate inductance L_g sets the series resonance frequency given as

$$\omega_0 = \sqrt{\frac{1}{(L_s + L_g)\,C_{gs}}} \tag{5.3}$$

The noise figure of the LNA can be calculated analyzing the equivalent circuit shown in Figure 5.3. The resistance R_l models the loss of the inductor L_g, R_g

represents the gate resistance of the NMOS transistor, the channel thermal noise of the device is represented by $\overline{i_d^2}$, and the induced gate noise is represented by $\overline{i_g^2}$. The overlap capacitance C_{gd} is neglected to simplify the analysis.
The transconductance of the amplifier driven from a 50 Ω source will be evaluated

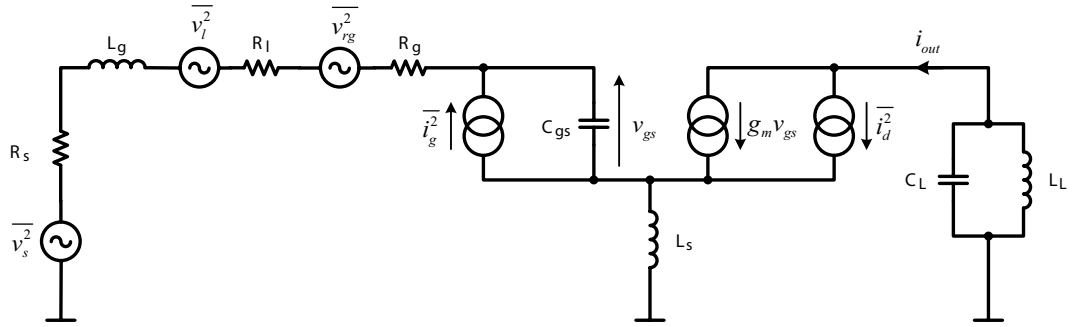


Figure 5.3: Equivalent circuit for noise calculation.

in order to calculate the output noise. The resistances R_l and R_g will be neglected in this evaluation as their values are small relative to the source resistance R_s. The following set of equations can be written for the above circuit:

$$v_{in} = i_{in}\left(Z_{in} + R_s\right) \tag{5.4}$$

$$v_{gs} = i_{in}\frac{1}{sC_{gs}} \tag{5.5}$$

$$i_{out} = g_m i_{in}\frac{1}{sC_{gs}} \tag{5.6}$$

The transconductance of the circuit can be defined as

$$G_m = \left|\frac{i_{out}}{v_{in}}\right| = \left|\frac{g_m}{sC_{gs}\left(R_s + Z_{in}\right)}\right| \tag{5.7}$$

When the input impedance is matched to the source impedance the effective transconductance is given by

$$G_m = \frac{g_m}{\omega_0 C_{gs}\left(R_s + \omega_T L_s\right)} = \frac{\omega_T}{\omega_0 R_s\left(1 + \frac{\omega_T L_s}{R_s}\right)} = \frac{\omega_T}{2\omega_0 R_s} \tag{5.8}$$

The noise factor utilizing the effects of induced gate noise evaluated for the circuit of Figure 5.3 is given by [Shaeffer 97]

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}\frac{\chi}{Q_L}\left(\frac{\omega_0}{\omega_T}\right) \tag{5.9}$$

where

$$\alpha = \frac{g_m}{g_{d0}} \tag{5.10}$$

$$Q_L = \frac{\omega_0 (L_s + L_g)}{R_s} = \frac{1}{\omega_0 R_s C_{gs}} \tag{5.11}$$

$$\chi = 1 + 2|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}\left(1 + Q_L^2\right) \tag{5.12}$$

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}} \tag{5.13}$$

and γ and δ are channel thermal noise and gate noise coefficients, respectively. Equations (5.8) and (5.8) indicate that the performance of the common-source LNA degrades as the operating frequency approaches the transistor's cut-off frequency ω_T since F and G_m are proportional to ω_0 and $1/\omega_0$ respectively.

Common-Gate LNA.

In the common-gate LNA the input signal is fed into the source of the transistor as shown in Figure 5.4. The gate of the transistor is tied to ground through the capacitor C_{bypass} to provide proper biasing and keeping the gate on ground for AC signal. The parasitic gate-source and gate-drain capacitances of the transistor are absorbed by the input matching network and the load LC tank and resonated out. Therefore, to the first order the performance of the common-gate stage is independent on the frequency. Using the small-signal model shown in Figure 5.5

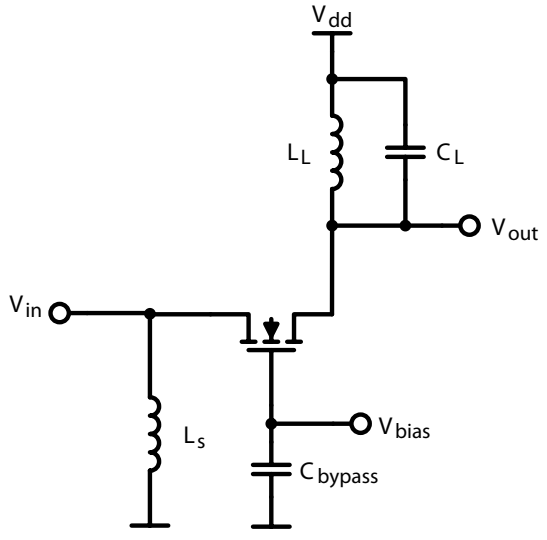


Figure 5.4: Common-source amplifier with inductive degeneration.

the input impedance can be calculated. The analysis takes into account the effect of finite transistor output resistance r_{ds}, which for short-channel MOS transistors is small. In common-gate amplifier the resistor r_{ds} forms a positive feedback between the input and output of the amplifier increasing the input impedance.

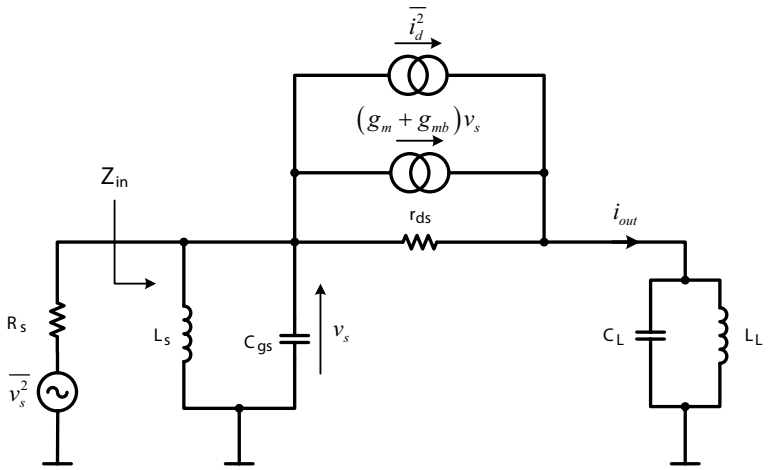


Figure 5.5: Small-signal equivalent circuit of the common-gate amplifier.

Applying nodal analysis to the small-signal circuit the input impedance can be expressed as

$$Z_{in} = \frac{r_{ds} + Z_L}{1 + (g_m + g_{mb})\, r_{ds} + \frac{r_{ds}+Z_L}{Z_s}} \tag{5.14}$$

where Z_s and Z_L represent the impedance of the input and output resonant LC tanks respectively. If the input and output LC tanks are at resonance the input impedance is given by

$$Z_{in} = \frac{r_{ds} + R_L}{1 + (g_m + g_m b) r_{ds}} \tag{5.15}$$

where R_L is equivalent shunt resistance introduced by a finite quality factor of the resonant load.
Noting that at resonance the input and output currents of the amplifier are equal and if the input impedance of the amplifier is matched to the source resistance R_s the transconductance can be written as

$$G_m = \frac{1}{2R_s} \tag{5.16}$$

The noise figure calculated for input match ($R_{in} = R_s$) is given by [Guan 02]

$$F = 1 + \frac{\gamma}{\alpha}\left(\frac{1}{1+\kappa}\right)\left(\frac{r_{ds}}{r_{ds}+R_L}\right) \tag{5.17}$$

where κ is the ratio of the backgate transconductance to that of the MOS transistor (g_{mb}/g_m). The above formula shows that the noise figure of a common-gate amplifier is not lower bounded by 2.2 dB if the effect of finite r_{ds} is taken into account.
If the drain current,I_D, is given the resistance r_{ds} can be substituted by $r_{ds} = \lambda\, I_D$

and the noise expression can written as

$$F = 1 + \frac{\gamma}{\alpha}\left(\frac{1}{1+\kappa}\right)\left(\frac{1}{1+R_L\lambda I_D}\right) \tag{5.18}$$

The above equation indicates that the reduction of the noise figure can be achieved by increasing power consumption of the amplifier and by improving the load resonant network.
The noise factor analysis does not account for transistor gate noise. However, the induced gate noise originates from the capacitive coupling between the gate and the channel [Shaeffer 97]. Since in a common-gate stage the coupling capacitance is resonated out at the frequency of operation the gate noise contribution to the overall performance seems to be negligible.

ESD protection.

One of the main bottlenecks for introducing CMOS RF devices to the market is their susceptibility to ESD. This is due to both gate oxide breakdown and junction degradation related problems, caused by decreased oxide thickness and increased doping levels in new short-channel CMOS technologies. The ESD protection becomes a severe problem in case of the RF circuits because of a strong influence of ESD devices on their performance.
Since the LNA is the first component in the receiver chain its input is connected to the outer world and has to sustain ESD stress that can be transfered from a human body defined by Human Body Model (HBM) [Ker 01]. The HBM consists of a 100 pF capacitor and a 1500 Ω series resistor as shown in Figure 5.6. The waveform specification of a HBM ESD pulse, generated by the ESD HBM tester to a short is presented in Figure 5.7. Commercial ICs are required to sustain at least 2 kV HBM ESD stress, which generate an ESD current peak of 1.3 A with a rise time of 10 ns.

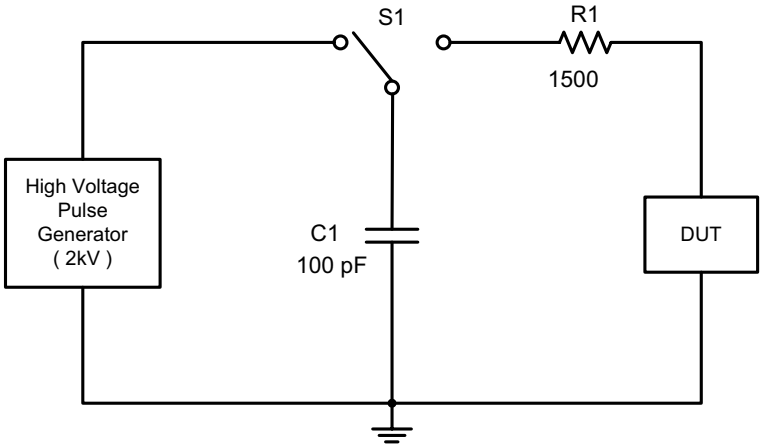


Figure 5.6: Equivalent circuit of a HBM.

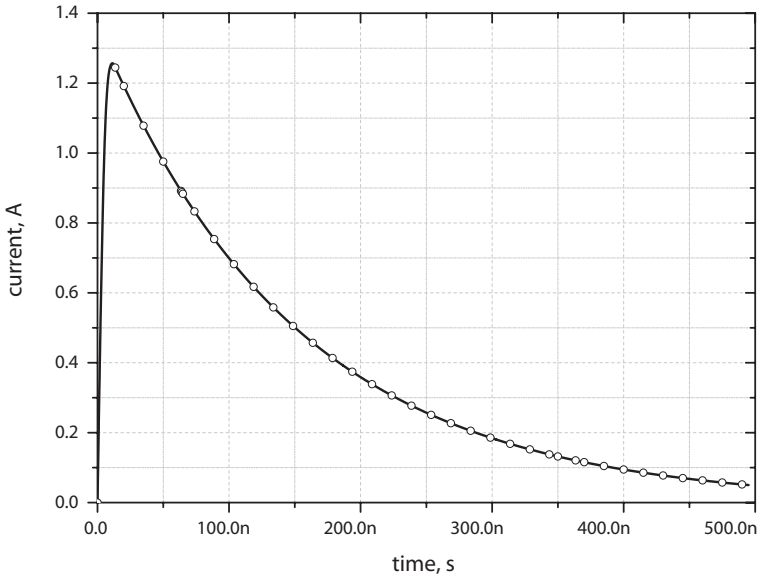


Figure 5.7: HBM ESD pulse current versus time.

Having the ESD requirements the capability of the CS and CG amplifiers to handle ESD pulses at the input has to be investigated. As shown in Figure 5.8 a) the input of a CS amplifier is connected to the gate of the transistor through the inductor L_s. An ESD pulse of 2 kV appearing at the gate of the transistor leads to the damage of the transistor, because the ESD voltage exceeds the breakdown voltage of the thin gate oxide. This shows that the CS amplifier has no ESD protection mechanism and additional circuitry has to be implemented to protect the input of the amplifier.

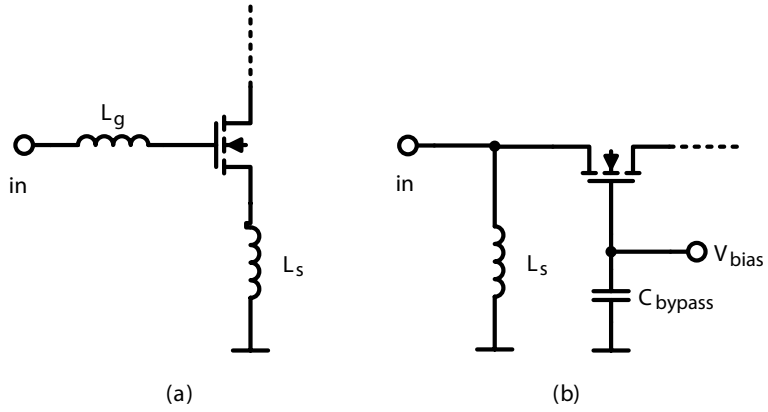


Figure 5.8: a) common-source and b) common-gate LNA inputs.

There have been many different ESD protection structures developed for CMOS technology [Wang 05]. However, they feature large parasitic capacitance and re-

sistance and cannot be applied in LNAs operating at high frequencies [Leroux 05]. ESD protection circuits for high frequency applications feature large size and have destructive influence on the performance of the LNAs [Linten 05], [Hyvonen 05], [Salerno 05].
In contrast to the CS amplifier, the input of the CG stage is tied down to ground by inductor L_s, as shown in Figure 5.8. The inductor L_s is a part of the input matching network, and provides low impedance path to ground for low frequency signals. The series resistance of this inductor defines the voltage which will be applied to the transistor. From ESD standpoint, the series resistance of the inductor should be minimized to minimize the voltage applied to the transistor. On the other hand, from the RF standpoint, this resistance defines the quality factor of the input matching and should be minimized in order not to degrade the noise performance of the LNA. This shows that the design goals for the input matching inductor are in agreement with both, ESD and RF design requirements.
The above discussion indicates that the CS amplifier needs an additional circuitry in order to provide the ESD protection of its input, and this circuitry has negative influence on the performance of the amplifier. On the other hand, in case of the CG amplifier the ESD protection is provided by the shunt inductor being a part of the input matching network.

Summary

Table 5.1 summarizes the performance of the two investigated amplifier configurations. The CS amplifier requires two inductors for input matching network. The

Table 5.1: Performance summary of the common-source and common-gate amplifiers.

	Common-Source Amplifier	Common-Gate Amplifier
Input Impedance	$Z_{in} = s\left(L_g + L_s\right) + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}}L_s$	$Z_{in} = \frac{r_{ds}+Z_L}{1+(g_m+g_{mb})r_{ds}+\frac{r_{ds}+Z_L}{Z_s}}$
Trans-conductance	$G_m = \frac{\omega_T}{2\omega_0 R_s}$	$G_m = \frac{1}{2R_s}$
Noise Figure	$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}\frac{\chi}{Q_L}\left(\frac{\omega_0}{\omega_T}\right)$	$F = 1 + \frac{\gamma}{\alpha}\left(\frac{1}{1+\kappa}\right)\left(\frac{1}{1+R_L\lambda I_D}\right)$
ESD protection	extra circuitry	built-in

equations defining the transconductance and the noise figure indicate the performance of the CS LNA degrades as the operation frequency becomes comparable

to ω_T. Additionally, for product-oriented applications extra ESD protection circuitry is needed which degrades the performance of the amplifier.
The CG gate amplifier employs single inductor in the input matching network. It is used to resonate out the parasitic capacitance. Additionally, it protects the input of the amplifier from high voltage ESD pulses by providing low impedance path to ground. The transconductance of the amplifier is independent on the frequency to the first order and it is comparable to the transconductance of the CS stage at high frequencies. The noise figure of the CG amplifier can be controlled by changing the drain current which can be a very important feature for an adaptive receiver concept.
Additional to the choice of the amplifier topology additional principles leading to a good LNA design should be considered:

- The transistors should be laid out with multiple gate fingers to reduce the total polysilicon gate resistance, and guard rings (substrate contacts) should be used to reduce the effective back-gate resistance
- The design of the inductors needed for input matching and load tanks should account for best quality factor and DC current driving capabilities, [Park 98]. Therefore, for high frequency application where the high modeling accuracy is required the usage of electro-magnetic simulators like Agilent Momentum [Momentum 07] or HFSS [HFSS 07] is essential.
- The use of cascode stages leads to improvement in gain and stability of an amplifier due to the elimination in the interaction between the input matching and the output matching circuits. Cascoding is proved to be an effective technique for reducing the Miller capacitance and is commonly used in amplifiers employing CS as the input stage.

5.2.2 5 - 6 GHz LNA implementation

Taking into consideration the performance analysis of different amplifier stages a common-gate differential architecture was chosen for the LNA. Even though, the current consumption and circuit complexity of a differential configuration are higher than in case of single-ended counterpart, the differential configuration gives the following benefits:

- doubling the available voltage swing - since the voltage swing is distributed to both equally loaded transistors, the dynamic ranges of the input and output signals are doubled through the superposition in comparison to single-ended structure
- high immunity to substrate noise and crosstalk - the common mode noise caused by substrate coupling or propagated over supply lines is rejected, also the immunity to crosstalk effects along the signal lines between the different circuit blocks is increased
- virtual ground on-chip - the grounding considerations of the chip are relaxed as a virtual on-chip ground is formed by the circuit symmetry, the circuit is more robust to the impact of the bond wires

The schematic of the implemented LNA is shown in Figure 5.9. The amplifier employs a transformer in the load circuit. Such solution enables DC separation between the amplifier and the following stages.

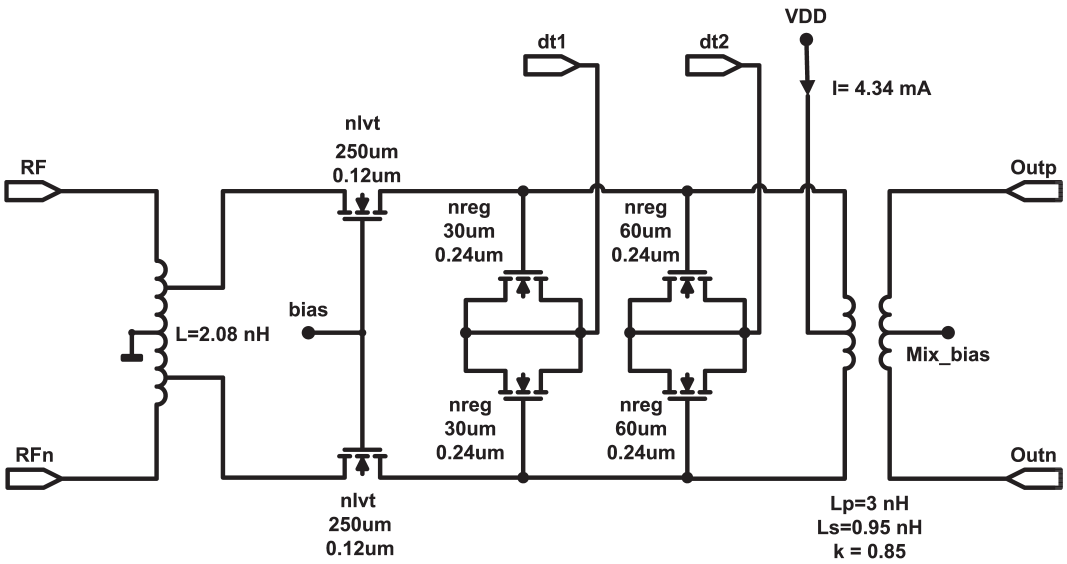


Figure 5.9: Simplified schematic of the implemented LNA.

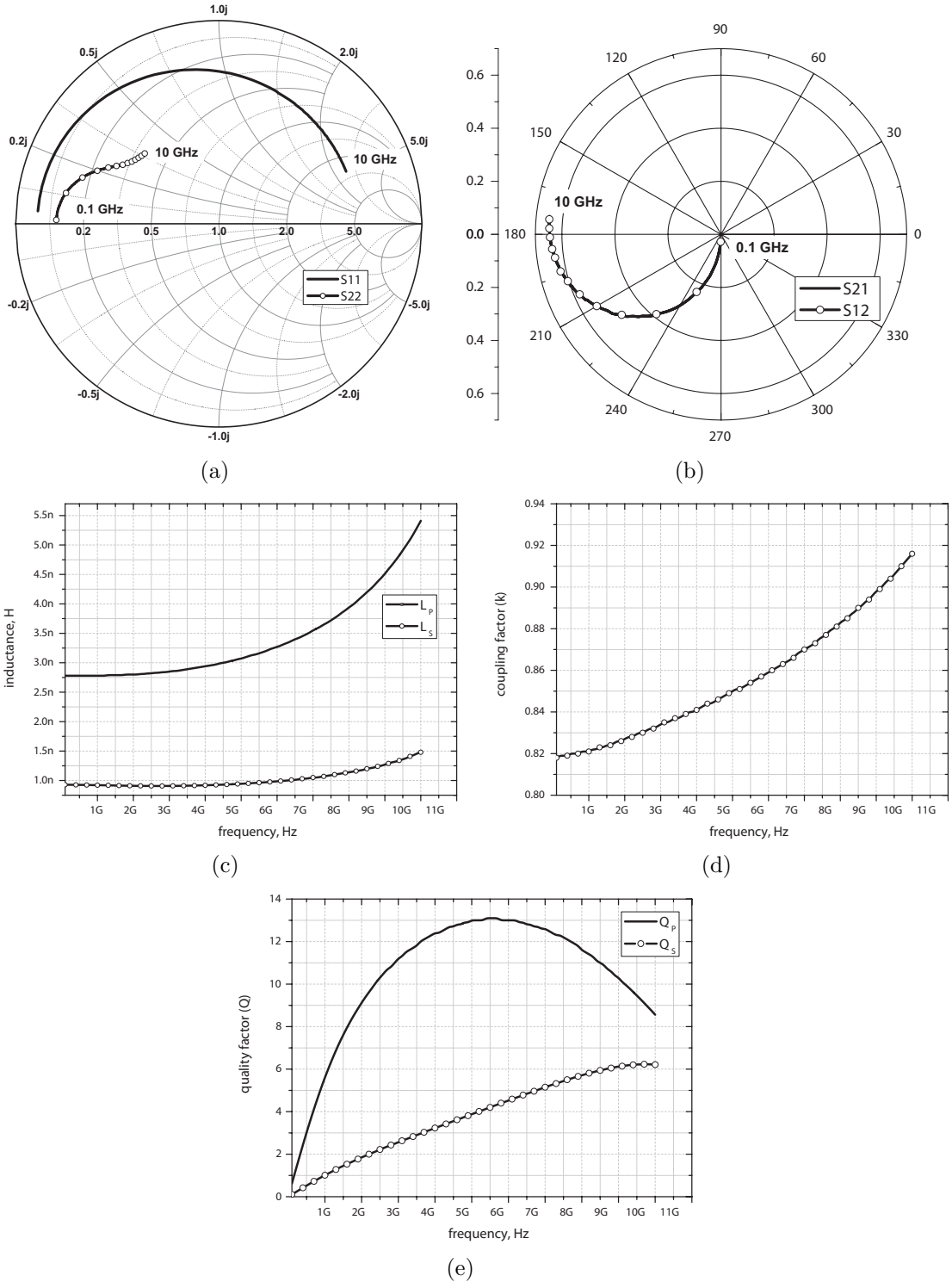
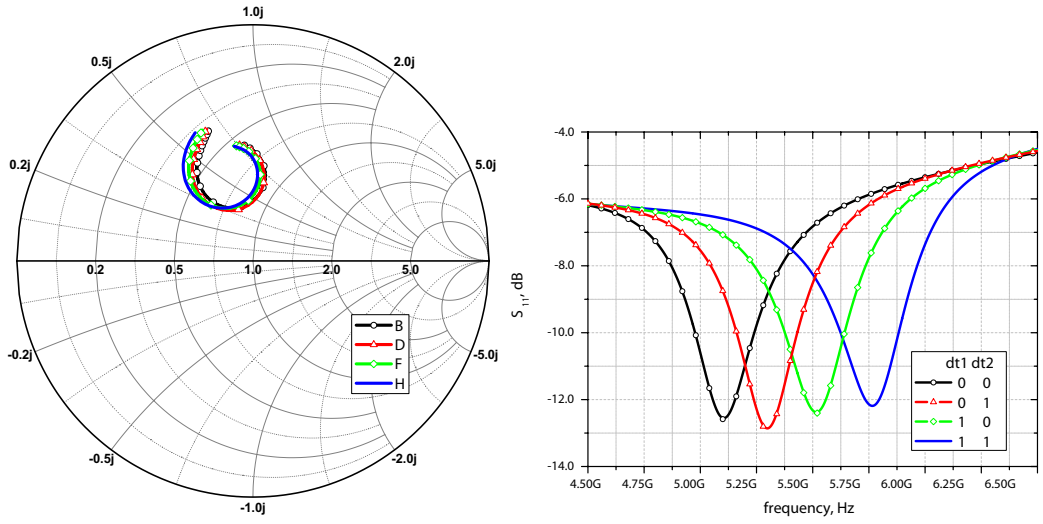


Figure 5.10: Simulated parameters of the load transformer: a) S11, S22; b) S12, S21; c) primary and secondary winding inductance; d) coupling factor; e) primary and secondary winding quality factor.

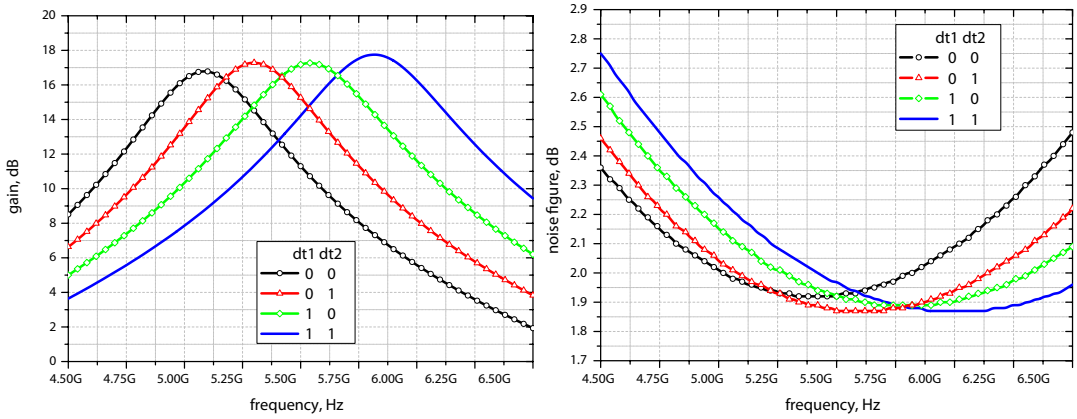
The transformer is realized as a broadside coupled structure. The primary (L_p) and secondary (L_s) inductances are 3.05 nH and 0.95 nH. The coupling coefficient of the transformer equals 0.85. The transformer with broadside coupling between the primary and the secondary winding features an area effective structure and is feasible for LNA where the DC current driving capabilities are relaxed. The transformer performance has been estimated using 2.5D Momentum simulator, [Momentum 07]. The simulated S-parameters of the transformer are shown in Figure 5.10 a) and b). The simulated inductances of the primary and secondary winding, their quality factors and coupling coefficient are presented in Figure 5.10 c), d) and f).
The multi-band operation requires an implementation of an amplifier which covers the frequency range from 5 - 6 GHz. Since the LNA is not required to cover the whole band at the same time it is possible to realize a narrow-band LNA with tunable frequency characteristics. The tunability of the frequency response is achieved by the application of four NMOS varactors in the load circuit of the amplifier serving as tunable capacitors. The size of NMOS varactors was adjusted to 35 μm and 70 μm, respectively, and applying DC voltage to inputs *dt1* and *dt2* enables the tuning of the capacitance of the varactors. Using digital DC signals to control the NMOS varactors the transfer characteristic of the amplifier can be tuned to four different center frequencies.
The input matching network consists of a tapped inductor and shunt capacitors. The usage of the tapped inductor introduced an extra variable in the input matching network. The position of the tapping is adjusted to resonate out the parasitic capacitance of the transistor, while the whole inductance is used to provide the match to 50 Ω. Due to the feedback between input and output of the common



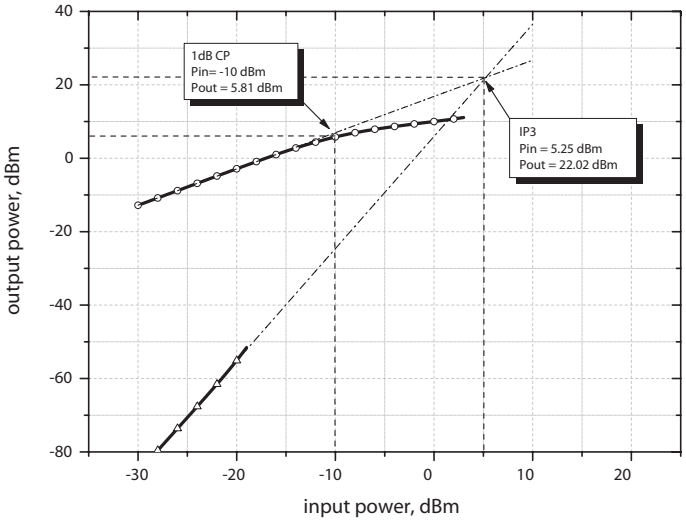
(a) (b)

Figure 5.11: Simulated insertion loss of the LNA.

gate amplifier formed by the resistance r_{ds} the input impedance is affected by the output impedance. This phenomenon simplified the design of a tunable amplifier, because there is no need to introduce separate tuning components for input matching network. The simulation results of the insertion loss of the LNA presented in Figure 5.11 show that the input impedance is tuned in the same way as the load impedance of the amplifier. The influence of the load impedance on the input matching is strong enough to provide $S_{11} < -12\,dB$ for all tuning settings. The simulated gain and noise figure of the LNA are presented in Figure 5.12 a) and b). The LNA exhibits a peak gain of 17 dB and tunable frequency characteristics yielding in the overall 3 dB bandwidth of more than 1 GHz. The simulated noise figure of the LNA is lower than 1.9 dB in the whole frequency range. The



(a) Gain (b) Noise Figure

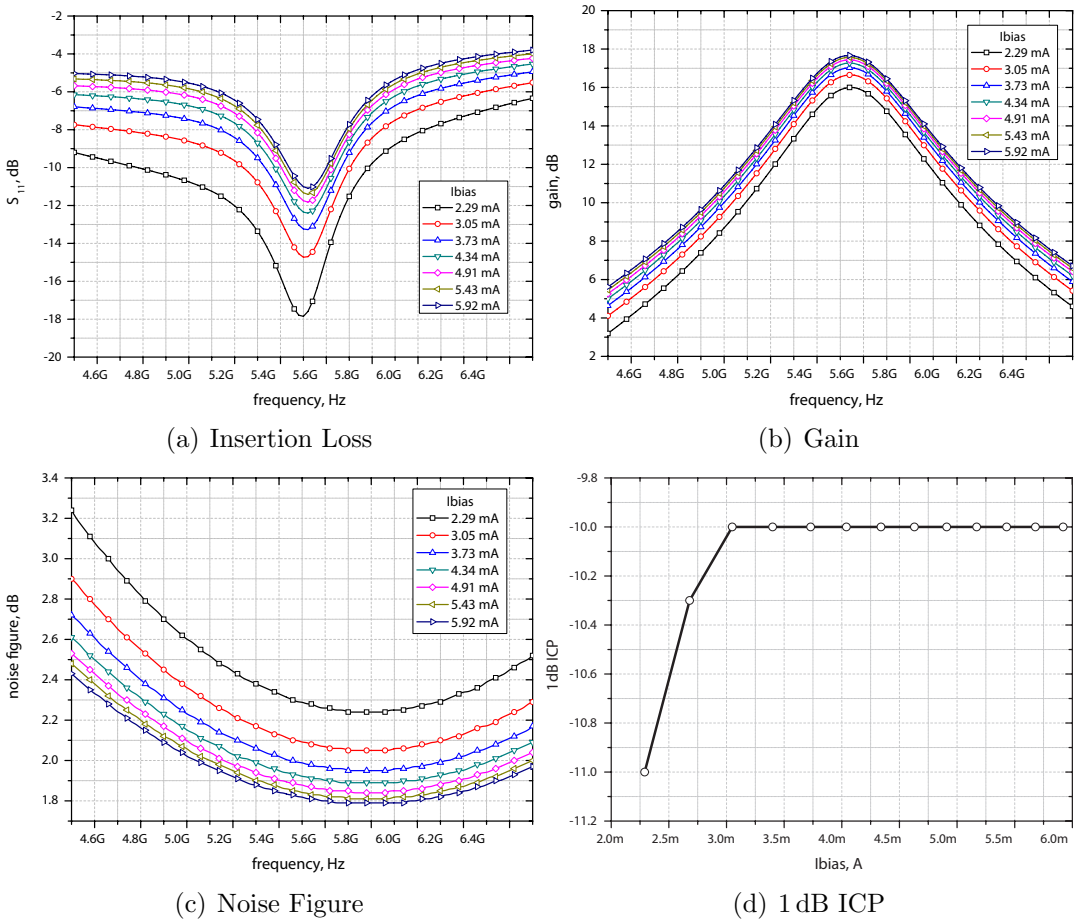


(c) Linearity at 5.5 GHz

Figure 5.12: Simulation results of the LNA.

simulation results of a two-tone test are shown in Figure 5.12 c). The amplifier reaches the 1 dB compression point at the input power of -10 dBm, and the in-

put IP3 at the input power of 5.25 dBm. The simulations were performed for the amplifier consuming 4.3 mA from a 1.5 V supply.
Since the amplifier is to be a part of a receiver with adaptive power consumption its feasibility to operate at different bias conditions should be also investigated. Figure 5.13 presents the main parameters of the LNA simulated for the bias current deviating ±50 % from the nominal value of 4.3 mA. The simulation results show that the insertion loss of the amplifier is decreasing as the bias current increases, however, it remains below -11 dB for all swept values. The gain of the amplifier changes by ±1 dB for minimum and maximum swept bias current values. The noise figure reaches 2.25 dB for the bias current reduced to 2.3 mA and decreases to 1.8 dB as the bias current is set to 5.9 mA. The input 1 dB CP drops by 1 dB for the lowest bias current and remains constant for all other swept values.
The simulation results show acceptable performance of the LNA under different bias conditions, proving the feasibility of the common gate amplifier for an adaptive receiver.



(a) Insertion Loss (b) Gain

(c) Noise Figure (d) 1 dB ICP

Figure 5.13: Simulated performance of the LNA for different biasing conditions.

The layout of the designed amplifier is shown in Figure 5.14. The transistors are laid out in multi-finger structures with the finger length of 5 μm. This reduces the series resistance of the polysilicon gate and minimizes its contribution to the noise of the amplifier. Additionally, the transistors are surrounded by guard rings (substrate contacts) which reduces the back-gate resistance. The NMOS varactors have also multi-finger structures to reduce their series resistance. The input tapped inductor has an octagonal shape. It employs three stacked top metalization layers which reduces the series resistance. The load transformer is implemented as a broadside coupled structure. The primary winding is realized in the top thick metalization, the secondary winding consists of two stacked metalization layers. The center tapping of the primary winding is connected to the V_dd, and the center tapping of the secondary winding is used to setup the biasing of the mixer. The amplifier occupies the chip area of 405 μm x 170 μm.

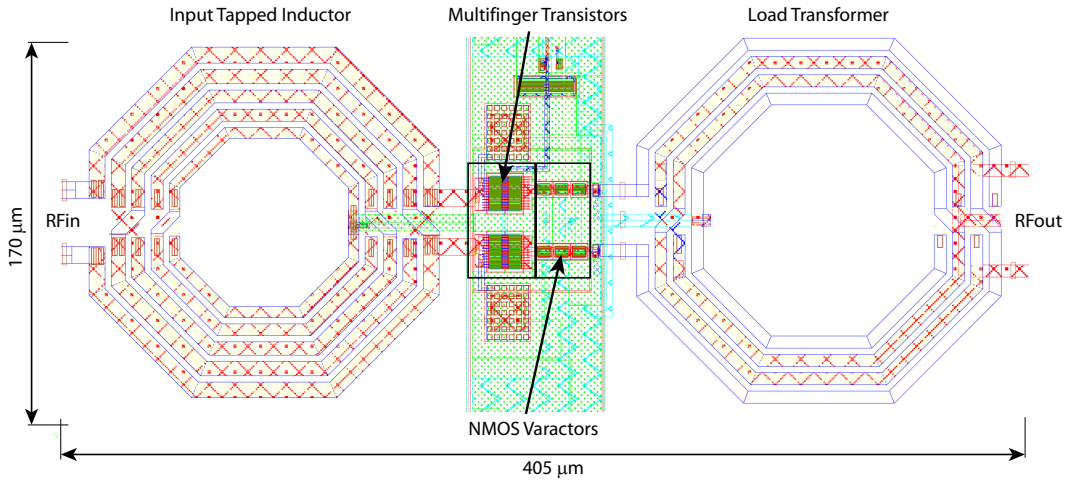


Figure 5.14: The layout of the LNA.

5.3 Down-Conversion Mixer

A RF front-end for wireless receiver is typically required to provide approximately 20 - 30 dB gain in order to limit the noise contribution of the analog baseband [Brandolini 05]. Since single stage LNAs deliver the gain in the order of 15 - 25 dB, the rest of the required gain is assigned to active mixers, which follow the LNAs in the receiver chain.
A down-conversion mixer for zero-IF receiver has to fulfill several requirements. First, it should contribute certain amount of gain to the receiver chain in order to suppress the noise of the following stages [Fong 99]. Additionally, it is desirable to optimize the noise performance of the mixer, as the low noise figure of the mixer reduces the gain requirements of the LNA. If the gain of the LNA can be reduced it is worth pointing out that the overall linearity of the receiver can be improved.
A down-conversion mixer aliases both the main and the image responses at the output. This must be considered when the mixer noise factor is specified. The single sideband (SSB) or double sideband (DSB) noise factor defines if the mixer output noise is referred to one or both input sidebands. The SSB noise factor is applicable to the heterodyne in which only one of the input RF sidebands is converted to the IF while the image band is rejected [Fong 99]. On the other hand, in a direct conversion receiver, the LO signal is centered in the desired channel and the desired signal and noise occupy the lower and upper sidebands [Rofougaran 96]. Therefore, in case of direct conversion receivers the DSB noise is applicable.
The mixer linearity often dominates the overall large signal performance of the RF front-end. The down-conversion mixer should feature adequately high ICP to handle large blocking or interferer signals which have negative influence on the sensitivity of the receiver. In addition to ICP, the mixer should feature sufficiently high IIP3. In down-conversion mixer, the third order modulation (IM3) may cause two large adjacent-channel signals to generate IM3 products which may coincident with the weak desired signal.
Integrated zero-IF receivers very often employ mixers based on single- or double-balanced topologies [Kivekas 01]. The mixers operating with differential LO signal and single-ended RF signal are referred as single-balanced. If a mixer accommodates both differential LO and RF signals it is called double-balanced. The double-balanced mixers provide better port-to-port isolation and they generate less even-order distortion that the single-balanced counterpart. On the other hand, the double-balanced topologies are more susceptible to noise in LO signal [Razavi 98]. Having in mind that the LNA delivers the differential signal to the mixer and taking the advantages of a differential circuit topology into account this thesis focuses on the double balanced mixer.
Most of the double-balanced mixers utilized in wireless receivers are based on the Gilbert mixer topology shown in Figure 5.15, [Gilbert 97]. The mixer structure can be divided into three stages: transconductance stage, switching stage and the

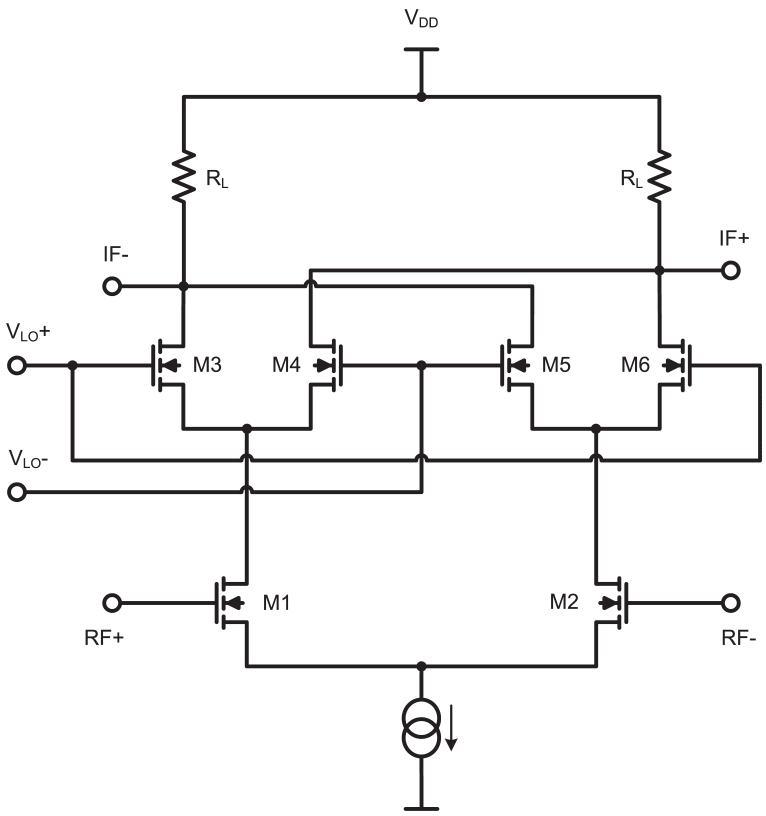


Figure 5.15: Gilbert double-balanced mixer.

output stage.The transconductance stage employs a differential pair *M1-M2* to convert the differential voltage-mode RF input signal to a differential current:

$$i_d(t) = G_m v_{in} \sin(\omega_{in} t) \tag{5.19}$$

where G_m is the transconductance of the input stage. The current-mode RF signal is then fed through the current switching quad *M3-M6* driven by the LO signal, which can be expressed as the multiplication with square signal:

$$i_{out}(t) = i_d(t) square(\omega_{LO} t) \tag{5.20}$$

The above multiplication of the RF signal with the square function realizes the frequency translation. If the LO signal is written as a Fourier series:

$$square(\omega_{LO} t) = \frac{4}{\pi} \sin(\omega_{LO} t) + \frac{4}{3\pi} \sin(3\omega_{LO} t) + \frac{4}{5\pi} \sin(5\omega_{LO} t) + \cdots \tag{5.21}$$

the multiplication with $\sin(\omega_{in} t)$ yields in new components in the output signal:

$$square(\omega_{LO} t) \sin(\omega_{in} t) = \frac{1}{2}\frac{4}{\pi} \cos[(\omega_{in} - \omega_{LO})t] + \frac{1}{2}\frac{4}{\pi} \cos[(\omega_{in} + \omega_{LO})t] + \cdots \tag{5.22}$$

where in the case of down-conversion the first term is the desired one, and all the others should be suppressed.
As the result of the multiplication the current-mode IF signal is obtained, which is then converted to the voltage at the output stage. If instantaneous switching of the switching quad is assumed (i.e. that the current-mode RF signal is multiplied by the square wave toggling at the LO frequency), the mixer voltage conversion gain is given by [Mahdavi 02]

$$A_v = \frac{2}{\pi} G_m R_L \tag{5.23}$$

The load of the mixer often consists of a first order RC low-pass filter which improves the mixer out-of-band blocking characteristics and relaxes the linearity requirements of the following baseband circuits. In case when the mixers are designed for heterodyne receivers or the IF frequency is high, the mixer is loaded with a parallel LC tank.
The noise and linearity of the mixer transconductance stage are crucial to the overall performance of the mixer. A MOS transistor can be modeled with [Rofougaran 96]

$$i_{DS} = \frac{K}{2}\frac{W}{L}\frac{(v_{GS} - V_T)^2}{1 + \theta(v_{GS} - V_T)} \tag{5.24}$$

where θ captures how the inversion layer mobility with the gate electric field. The *IIP3* of a down-conversion mixer employing common-source transconductance stage can be estimated by considering the *IIP3* of the common-source circuit, which can be approximated as [Sivonen 05]

$$v_{IIP3} = \frac{4}{\sqrt{3}}\sqrt{\frac{V_{eff}(2 + \theta V_{eff})}{\theta}}\,(1 + \theta V_{eff}) \approx 4\sqrt{\frac{2}{3}\frac{V_{eff}}{\theta}} \tag{5.25}$$

where $V_{eff} = V_{GS0} - V_T$, V_{GS0} is the bias voltage at the gates of *M1-M2* and the approximation holds if $\theta V_{eff} << 1$ [Sansen 99]. The equation (5.25) shows that the *IIP3* of the common-source transconductor scales up by increasing the V_{eff}. Additionally, the long channel transistors at the input improve the linearity, since θ is inversely proportional to the channel length. As the V_{eff} of the input transistors *M1-M2* defines the *IIP3*, the dimensions of the input transistors determine the transconductance of the input stage

$$g_m = \frac{K}{2}\frac{W}{L}\frac{(2 + \theta V_{eff})\,V_{eff}}{(1 + \theta V_{eff})^2} \approx \frac{2I_{DS}}{V_{eff}} \tag{5.26}$$

and the bias current I_{DS}. In order to provide tolerable DSB noise factor the g_m of the transconductance stage must be sufficiently large. The noise factor for the mixer shown in Figure 5.15 is given by [Darabi 00]

$$F_{DSB} = \frac{\pi^2}{8}\left(1 + \frac{\gamma}{g_m R_S} + \frac{2\gamma I_{DS}}{g_m^2 R_S \pi A_{LO}} + \frac{1}{g_m^2 R_L R_S}\right) \tag{5.27}$$

The mixer conversion gain expressed as

$$A_v = \frac{2}{\pi} g_m R_L \approx \frac{2}{\pi} \frac{2I_{DS}}{V_{eff}} R_L \tag{5.28}$$

is required to be high enough to overcome the noise contribution from the mixer load (R_L) and the following baseband stages of the receiver. However, as the common-mode level of the mixer is given by $V_{OCM} = V_{DD} - I_{DS}R_L$, the DC voltage drop across the load resistors links the maximum obtainable gain with the supply voltage. Thus, for low values of the supply voltage the scaling of the gain by increasing the load resistors (R_L) or the bias current I_{DS} is limited to the point at which V_{OCM} is too low for the switching quad and the transconductance stage to remain in saturation. Therefore, the realization of a basic mixer operating at low supply voltage with reasonable amount of gain and fulfilling linearity and noise requirements is difficult.
In a direct conversion receiver, where the signal is down-converted to the baseband the mixer flicker noise can degrade the overall noise figure of the receiver. It is essential then to understand the contribution of the $1/f$ noise of each of the mixer stages. The transistors of the input transconductance stage contribute only white noise to the output [Darabi 05]. The noise of the load stage directly influences the down-converted signal, however, the usage of PMOS transistors may lower the flicker noise [Chang 94], [Binkley 02]. As an alternative, in expense of the voltage headroom, the mixer can be loaded with polysilicon resistors which are free of $1/f$ noise. The flicker noise of the switching stage appears at the output without a frequency translation [Darabi 00]. The switches in an active mixer contribute flicker noise to the output in two different ways. One way, referred as direct, is by random modulation of the time instants of the mixer switching which contributes the flicker noise at or near IF. The indirect mechanism models the flicker noise contribution when the mixer is driven by a square-wave LO waveform with infinite slope. In this case, the flicker noise induces current in the tail capacitance which is commutated to the output. In most practical applications the flicker noise arises from the direct mechanism since the mixer is driven by a sine-wave LO signal. The flicker noise current due to the direct mechanism is given by [Darabi 00]

$$i_{o,n} = 4I_{SW} \frac{v_n}{S \times T} \tag{5.29}$$

where I_{SW} is the bias current of each switching pair, v_n represents the equivalent flicker noise of the switching quad, S is the slope of the LO signal at the switching time and T is the period of LO signal equal to $2\pi/\omega_{LO}$. Thus, the flicker noise due to the direct mechanism can be minimized by increasing the slope of the LO signal, reducing I_{SW}, or by reducing the flicker noise of the switching transistors which leads to increase in their size.

The performance of a standard CMOS mixer can be improved by a current boosting technique as shown in Figure 5.16, [MacEachern 98], [Ryynanen 01]. The idea of this technique is to relax the low voltage operation, to decouple the mixer gain from the supply voltage, and to reduce the bias current of the switches (I_{SW}) which leads to lowering the flicker noise at the output. A part of the input stage

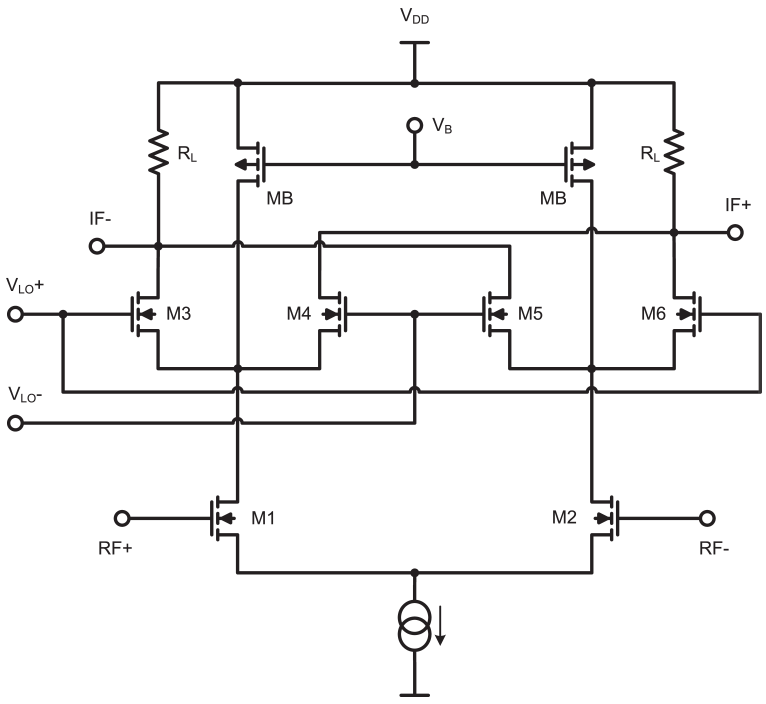


Figure 5.16: Double-balanced mixer with current boosting.

bias current I_{DS} is supplied by M_B which allows larger input stage g_m and R_L with transconductance and switching transistors operating in saturation. However, the white noise of the current source increases the overall noise figure of the receiver. The noise factor of the mixer with current boosting, utilizing the results derived in [Darabi 00] and [Terrovitis 99], can be approximated as

$$F_{DSB} = \frac{\pi^2}{8}\left(1 + \frac{\gamma_n}{g_m R_S} + \frac{2\gamma_n I_{DS}}{g_m^2 R_S \pi A_{LO}} + \frac{1}{g_m^2 R_L R_S} + \frac{\gamma_p g_{mB}}{g_m^2 R_S}\right) \tag{5.30}$$

where the last term denotes the channel thermal noise of M_B ($\overline{i_d^2} = 4kT\gamma_p g_{mB}\Delta f$), and γ_n and γ_p are the channel current noise factors of NMOS and PMOS transistors, respectively.
Thus the current source contributes white noise to the overall noise figure, however, the current boosting technique enables to achieve higher gain and lower noise figure without deteriorating the linearity than in a standard mixer topology. Therefore this mixer topology has been chosen for the implementation in this work.

The mixer with current boosting designed for integration in a direct-conversion 5 - 6 GHz receiver is shown in Figure 5.17. The mixer employs low-V_T transistors in the transconductance stage and in the switching quad to maximize the voltage headroom. The two PMOS transistors boost the current in the transconductance stage. The mixer is loaded with 525Ω polysilicon resistors which contribute no flicker noise to the output and allow to realize sufficient gain in the mixer. The mixer employs a stacked current mirror as the current source. Such current source features increased output resistance compared to a standard one, and by using low-V_T and regular V_T transistors it operates at low voltages which maximizes the voltage headroom for the transconductance stage. The simulated performance

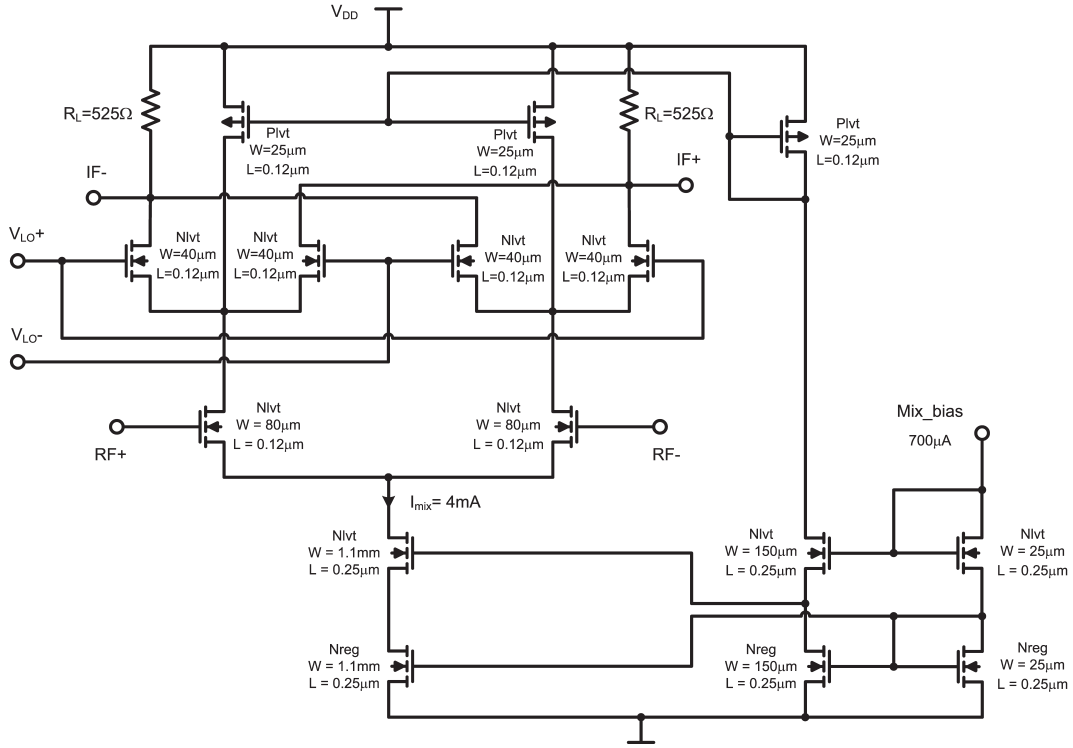
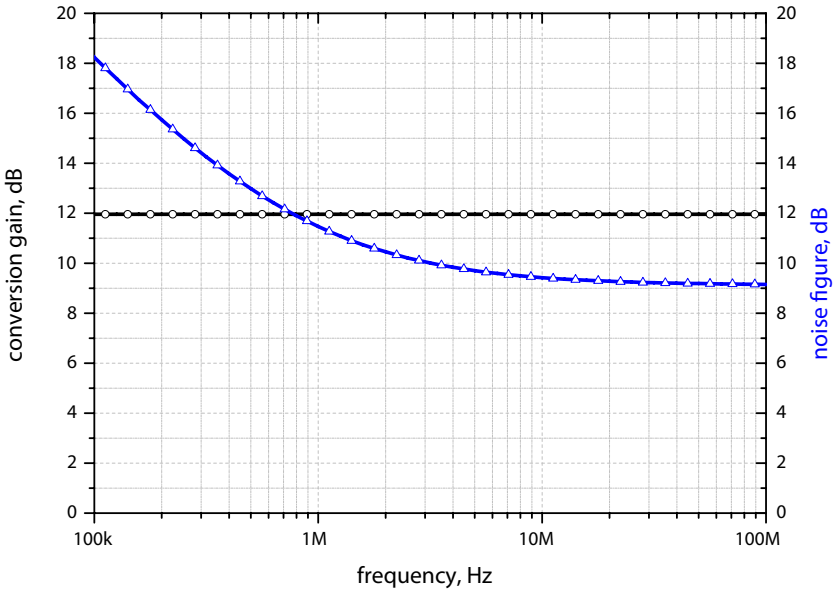
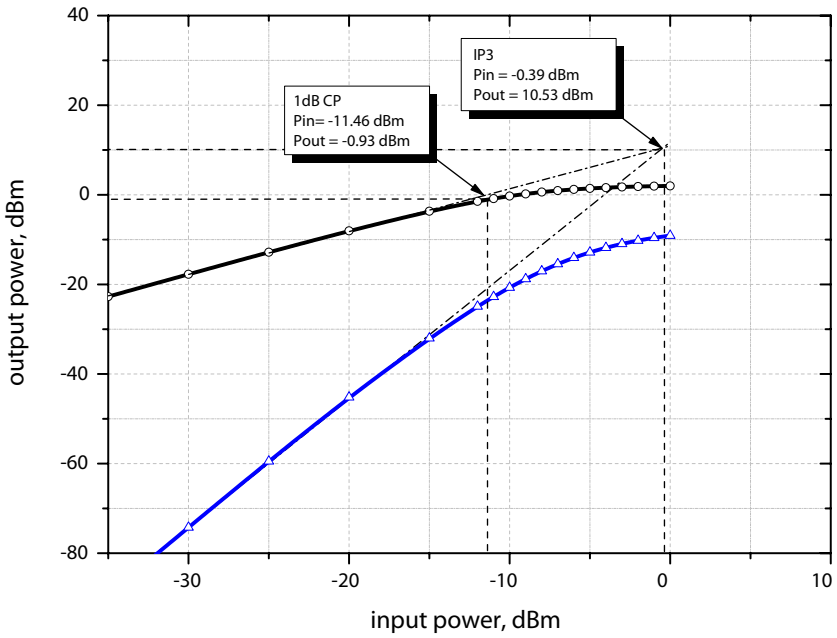


Figure 5.17: Double-balanced mixer with current boosting implemented in direct-conversion 5 - 6 GHz receiver.

of the mixer is presented in Figure 5.18. The mixer exhibits the conversion gain of 11.9 dB and noise figure of 9.5 dB in the frequency range of 1 - 100 MHz. The flicker noise raises the noise figure of the mixer at low frequencies leading to the noise figure of 18 dB at 100 kHz. However, according to the system simulations this performance is acceptable since the frequency range 0 -250 kHz will not be used. The linearity performance has been simulated employing a two-tone test. The applied two tones resulted in the IF signals at 24 and 26 MHz and produced third order intermodulation products at 22 and 28 MHz. The mixer reaches the 1 dB CP at the input power of -11.5 dBm and the IP3 at the input power of -0.4 dBm. The simulations were performed for the mixer driving the DC current of



(a) Conversion gain and noise figure



(b) Linearity at IF = 25 MHz

Figure 5.18: Simulated conversion gain, noise figure and linearity of the down-conversion mixer.

4 mA from a 1.5 V supply. Employing the current boosting, the transconductance stage is operating at the full bias current of 4 mA while the switches drive only half of the whole current. This enabled to achieve the needed gain while not deteriorating the linearity of the mixer.

5.4 Tunable BB Filter and PGA

The channel select filter and the PGA were designed with the help of other colleagues of our team and were used as ready components to complete the receiver, therefore only a brief overview will be presented.

Programmable Gain Amplifier

The schematic of the implemented differential programmable amplifier is presented in Figure 5.19. It employs a standard degenerated pair with resistive load [Hsu 03]. The differential input voltage signal v_{in} is copied over the series impedance of the two nonlinear transconductances g_m and the linear degeneration resistor R_D resulting in a differential signal current i_{ac} given by [Rijns 96]

$$i_{ac} = \frac{v_{in}}{R_D + \frac{2}{g_m}} \tag{5.31}$$

A major advantage of this architecture is that the amplifier can be designed to produce both gain and attenuation by means of changing the ratio of load an degeneration resistors. The variable degeneration resistors ensure that the poles

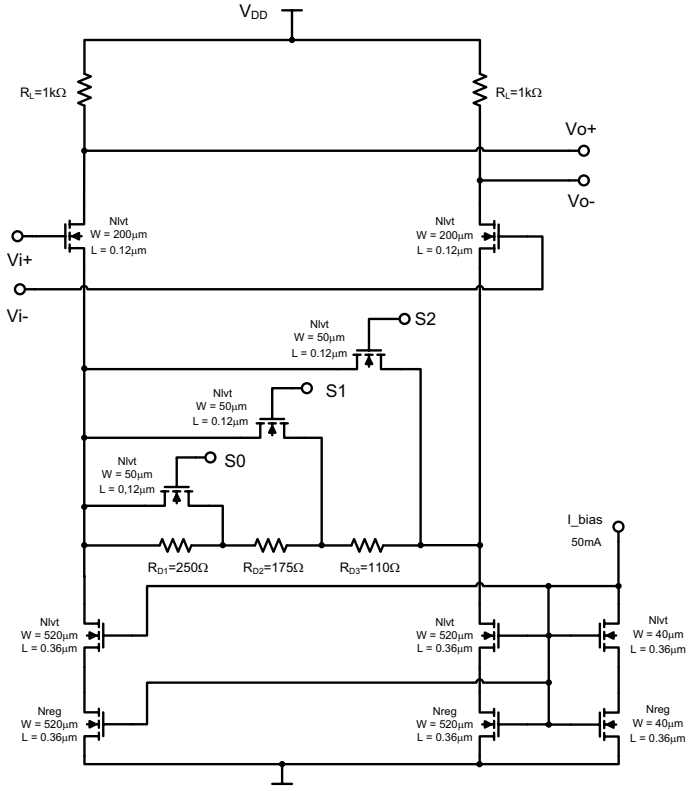


Figure 5.19: Schematic of the implemented PGA.

of the PGA output nodes are kept constant and therefore the bandwidth of the

amplifier is independent of the programmable gain [Rijns 96]. The variable degeneration resistor is implemented as a set of three resistors with CMOS switches which are controlled by inputs *S0-S2*. The load resistor of the amplifier was set to $1k\,\Omega$ and with degeneration resistors of $110\,\Omega$, $175\,\Omega$ and $250\,\Omega$ the amplifier delivers the gain of 6.3 dB, 9.3 dB, 12.4 dB and 15.3 dB which was the design goal. Additionally, according to the system planning, it was required to implement

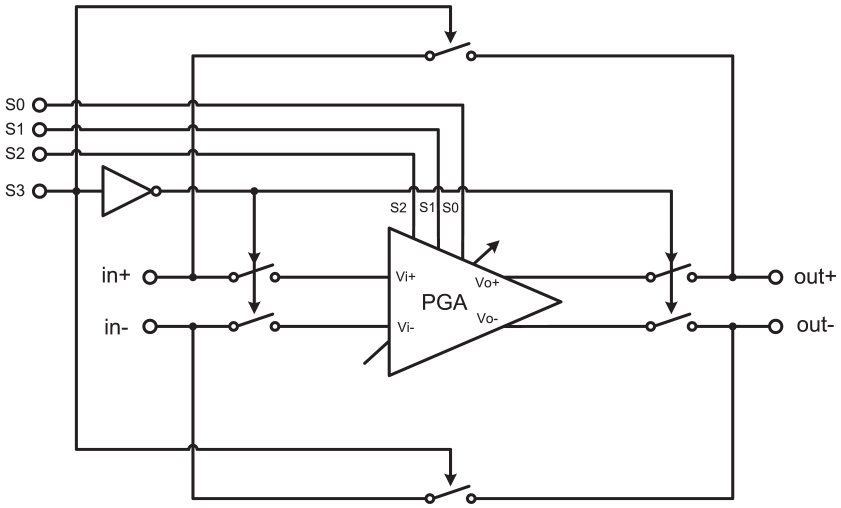


Figure 5.20: Schematic of the implemented PGA with bypass option.

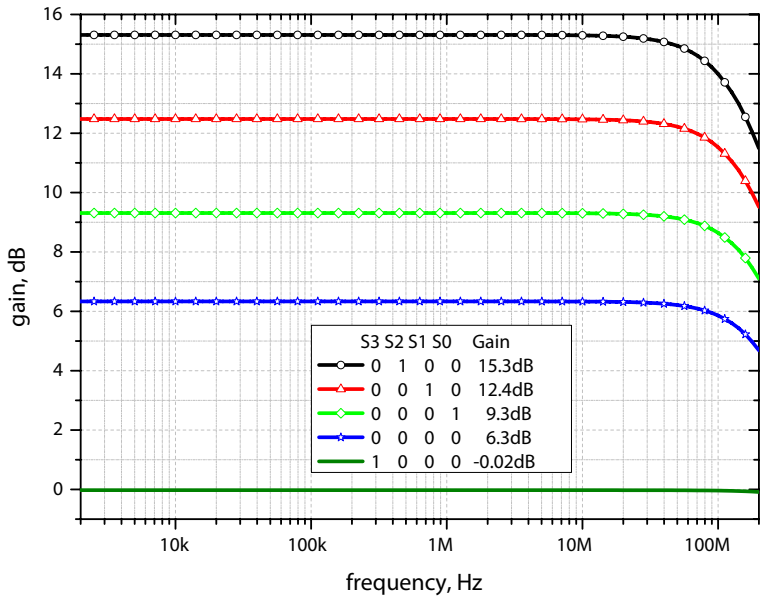


Figure 5.21: Frequency response of the PGA.

the possibility to bypass the amplifier. Therefore, the structure employing a set

of switches was implemented as shown in Figure 5.20. The simulated frequency response of the amplifier for all gain settings is presented in Figure 5.21.

Baseband Filter

The channel select filter is realized as a 6^{th} order Sallen-Key structure as shown in Figure 5.22. In order to implement the tuning of the corner frequency batteries of binary-weighted capacitors are used. The filter characteristic can be then

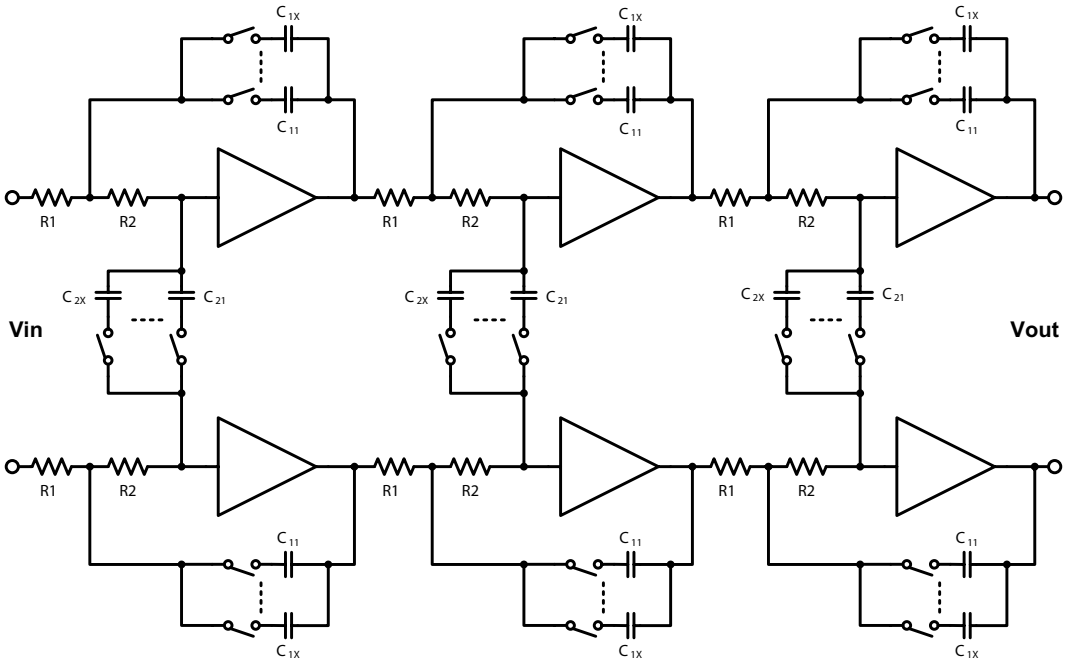


Figure 5.22: Schematic of the implemented BB filter.

controlled by switching certain amount of capacitors to obtain the desired cutoff frequency. The design goal for this filter was to obtain the 3 dB cutoff frequency tunable to the following values: 6.5 MHz, 10 MHz, 20 MHz and 50 MHz.
The basic block of the filter is a Sallen-Key biquad shown in Figure 5.23, [Johns 97]. It employs an opamp in an arrangement of voltage-controlled voltage source with gain G. This topology belongs to the enhanced positive feedback class of biquads employing single amplifier. The transfer function of the circuit is given by [Deliyannis 99]

$$H(s) = \frac{V_o}{V_i} = \frac{\frac{G}{C_1 C_2 R_1 R_2}}{s^2 + \left(\frac{1}{R_1 C_1} + \frac{1}{R_2 C_1} + \frac{1-G}{R_2 C_2}\right) s + \frac{1}{C_1 C_2 R_1 R_2}} \tag{5.32}$$

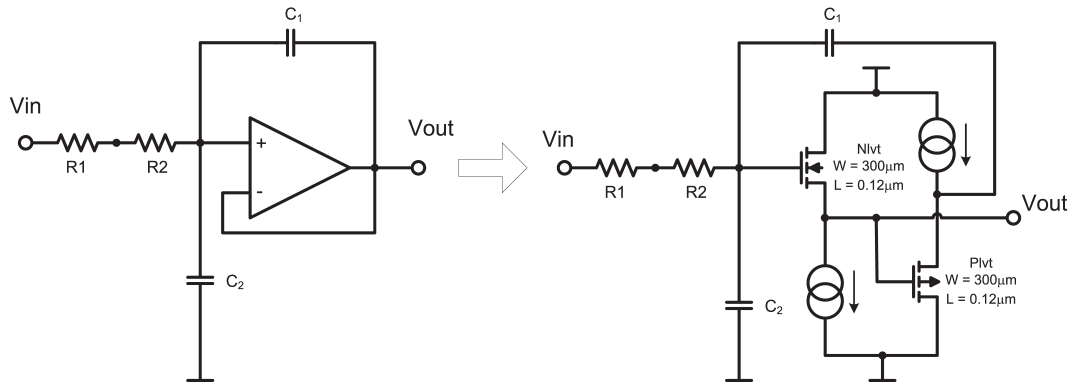


Figure 5.23: Implementation of the Sallen-Key biquad.

In order to realize the second-order lowpass function

$$F(s) = \frac{K}{s^2 + \beta s + \gamma} \tag{5.33}$$

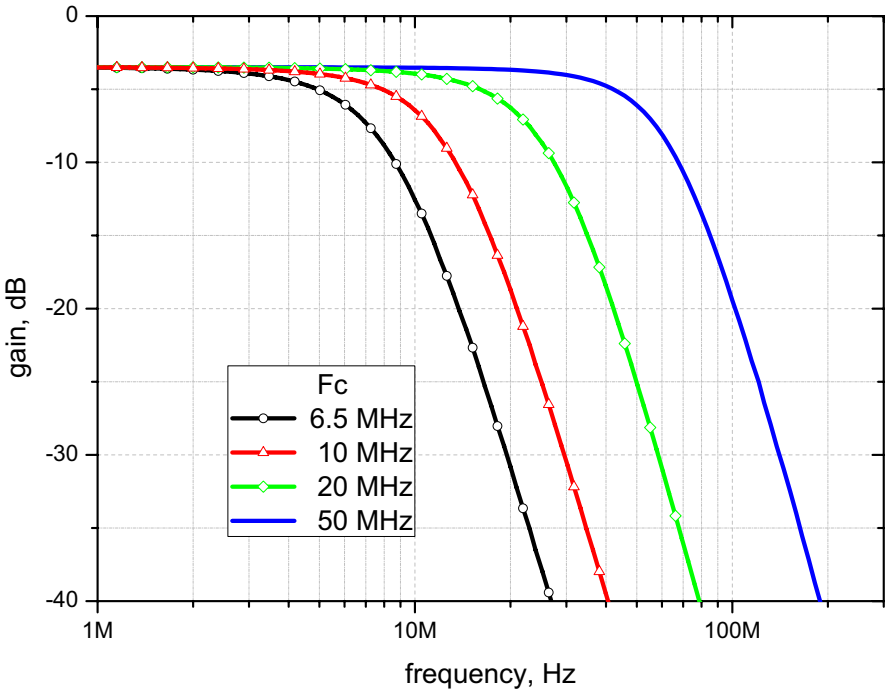
it is necessary to match the coefficients of the same powers which leads to the following relations:

$$\frac{1}{R_1 C_1} + \frac{1}{R_2 C_1} + \frac{1-G}{R_2 C_2} = \beta \tag{5.34}$$

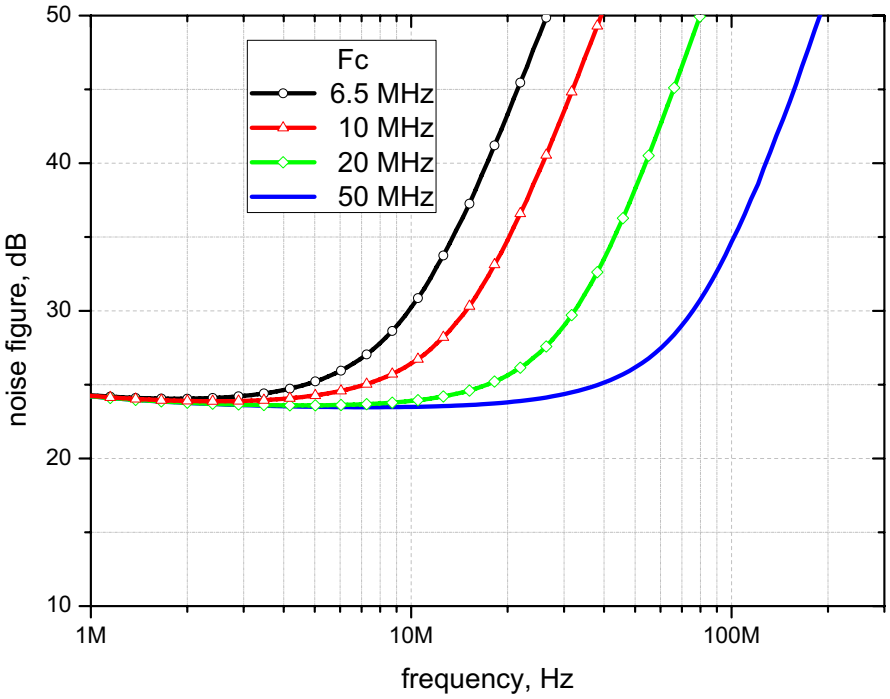
$$\frac{1}{C_1 C_2 R_1 R_2} = \gamma \tag{5.35}$$

$$\frac{G}{C_1 C_2 R_1 R_2} = K \tag{5.36}$$

The filter employs the amplifiers based on the source-follower topology. Thus, the filter features a 3.5 dB attenuation in the passband but the linearity performance is maximized. Due to the lack of gain in the buildings blocks of the filter the noise figure of the filter is high and its contribution to the overall receiver performance has to be minimized by placing a PGA in front of the filter. The frequency response of the filter for all adjustable corner frequencies with corresponding noise figures is shown in Figure 5.24.



(a)



(b)

Figure 5.24: Simulated a) gain and b) noise figure for all adjustable cutoff frequencies.

5.5 Power Detector

The concept of an adaptive receiver requires design of an analog preprocessing circuit. The goal of this circuit is to detect the input signal power and according to it adjust the gain of the PGAs. The block diagram of the designed analog preprocessing circuit is shown in Figure 5.25. The circuit consists of a power de-

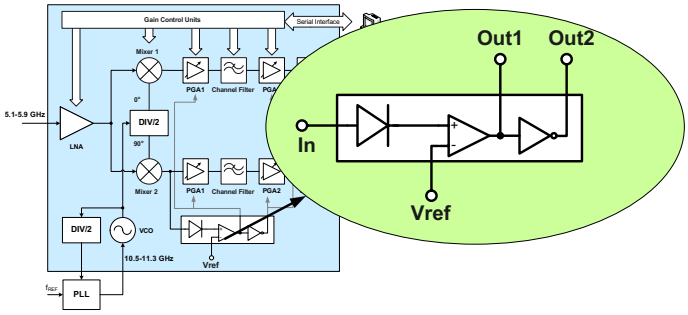


Figure 5.25: Block diagram of the analog preprocessing circuit.

tector, comparator and an inverter. The output signal of the power detector is compared with the reference voltage V_{ref} and according to the comparison the gain of the PGAs can be setup.

The power detector circuit is shown in Figure 5.26, [Treankle 01]. The circuit

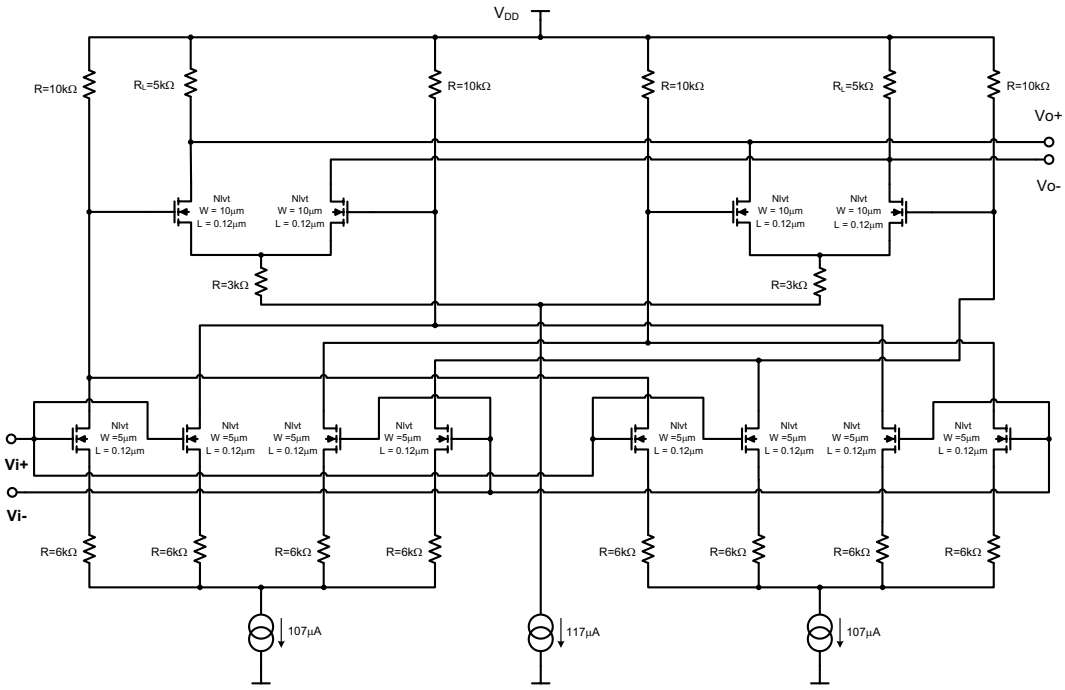
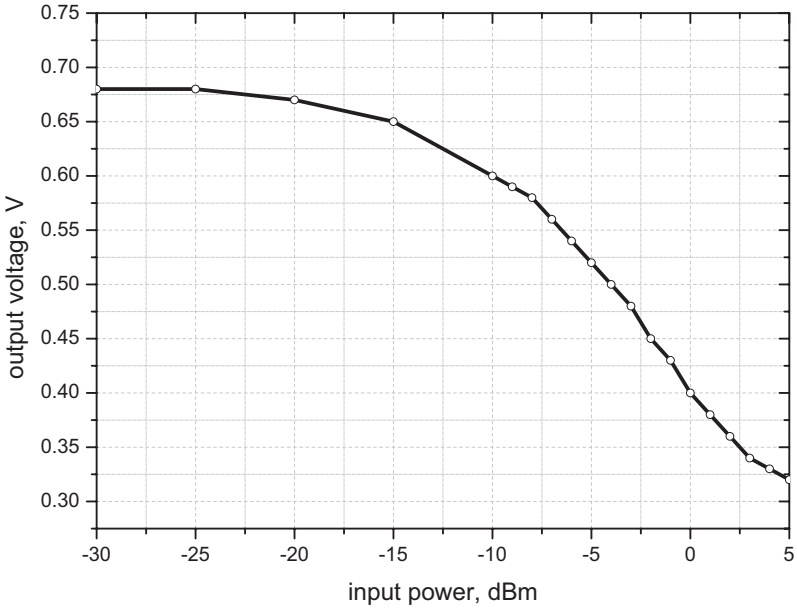
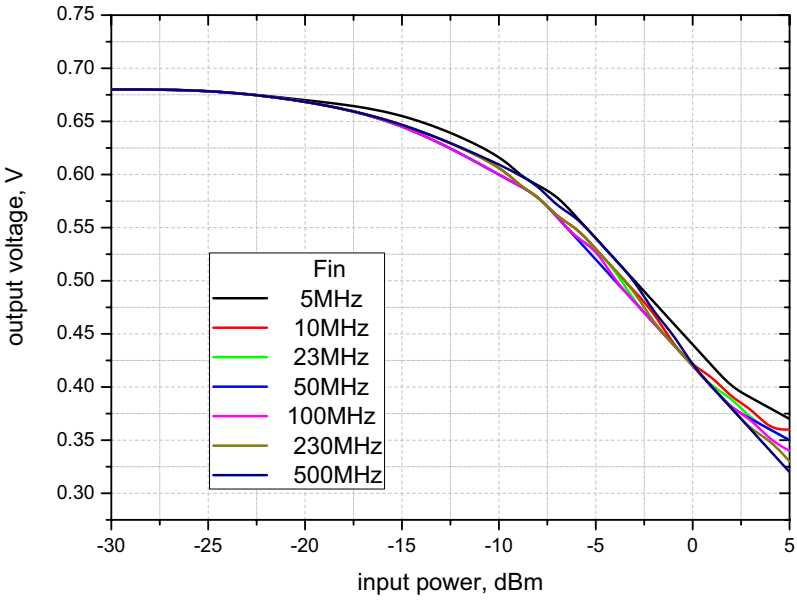


Figure 5.26: Schematic of the implemented power detector.

squares the input signal yielding in an output signal proportional to the power of the input signal. The circuit has two identical inputs, and therefore the output signal is free from errors caused by phase shifts. The power detector drives



(a)



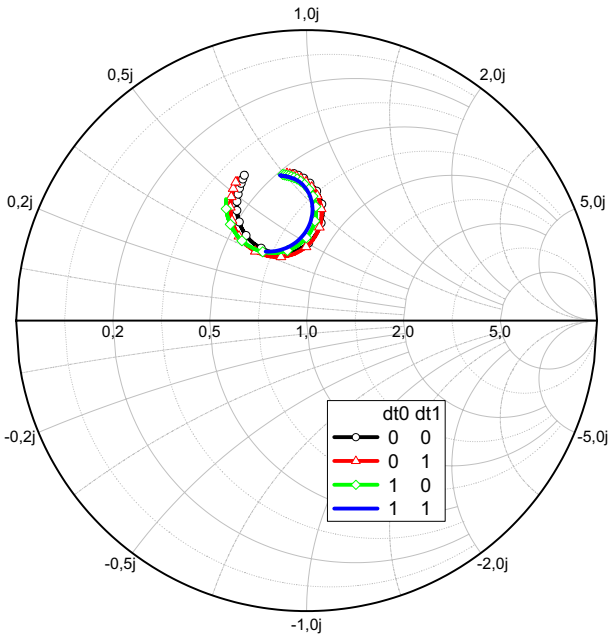
(b)

Figure 5.27: Simulated performance of the power detector a) for input signal frequency of 100 MHz, b) for input signal frequencies from the range 50 - 500 MHz.

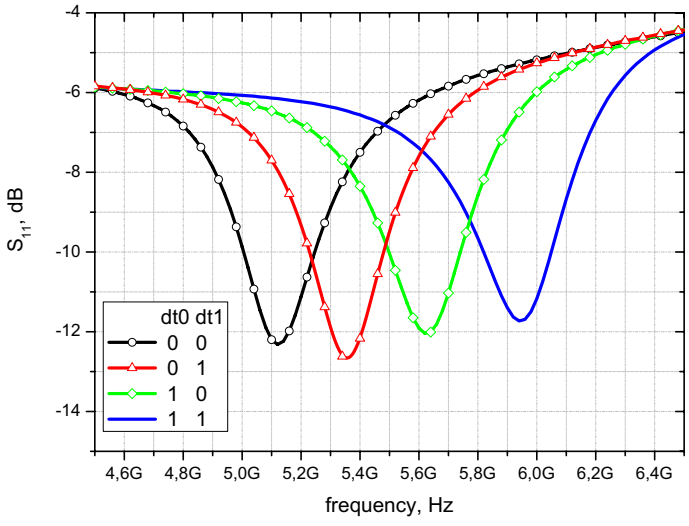
0.33 mA from a 1.5 V supply. The performance of the circuit illustrated in Figure 5.27 proves the capability of broadband operation of the circuit.

5.6 Simulated performance of the 5 - 6 GHz receiver with BB filter

Having each of the receiver building blocks designed the overall performance of the 5 - 6 GHz receiver is investigated. The insertion loss of the receiver shown in



(a)



(b)

Figure 5.28: Simulated insertion loss of the receiver.

Figure 5.28 reflects the tuning of the LNA between the needed bands of operation. The overall conversion gain and noise figure of the receiver is shown in Figure 5.29.

The receiver employs two PGAs with which we can adjust the chain gain. The settings of the gain influence the overall noise performance as well as the overall linearity. Figure 5.30 presents the frequency response of the receiver for different

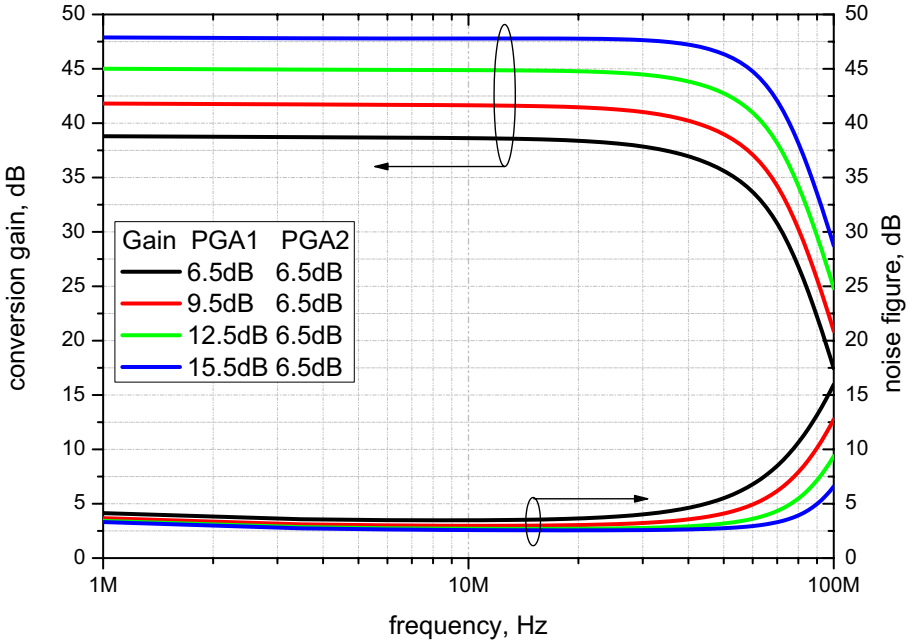


Figure 5.29: Simulated conversion gain and noise figure of the receiver.

settings of the cutoff frequency of the filter. This feature enables the multi-mode capability of the receiver.

Additionally, a fine-tuning of each cutoff frequency is implemented, as shown in Figure 5.31. This feature enables to compensate for component parameters variations which take place during the production process. The linearity of the receiver is dominated by the performance of the filter and the PGAs. Depending on the PGA settings the simulated receiver linearity is shown in Figure 5.32. The application of two PGAs was required in order to suppress the noise contribution of the filter. Figure 5.33 shows the influence of the PGAs settings on the overall noise performance of the receiver.
The performance of the receiver is summarized in Table 5.2.

Table 5.2: The overall performance of the receiver.

1 dB Bandwidth	4.9 - 6.1 GHz				
Overall Gain @ 25 MHz	26 dB	38 dB	41 dB	44 dB	47 dB
Noise Figure @ 25MHz	4.9 dB	3.8 dB	3.1 dB	2.7 dB	2.6 dB
Overall 1 dB ICP	-23 dBm	-36 dBm	-37 dBm	-38 dBm	-40 dBm
Power Consumption	122.5 mW @ $V_{DD} = 1.5\,V$				

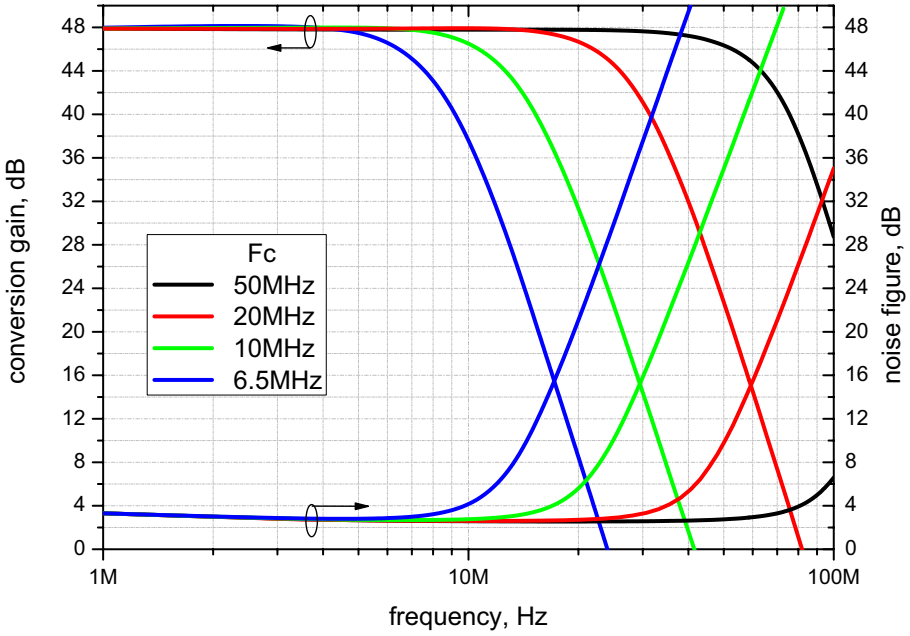


Figure 5.30: Channel select filter corner frequency tuning.

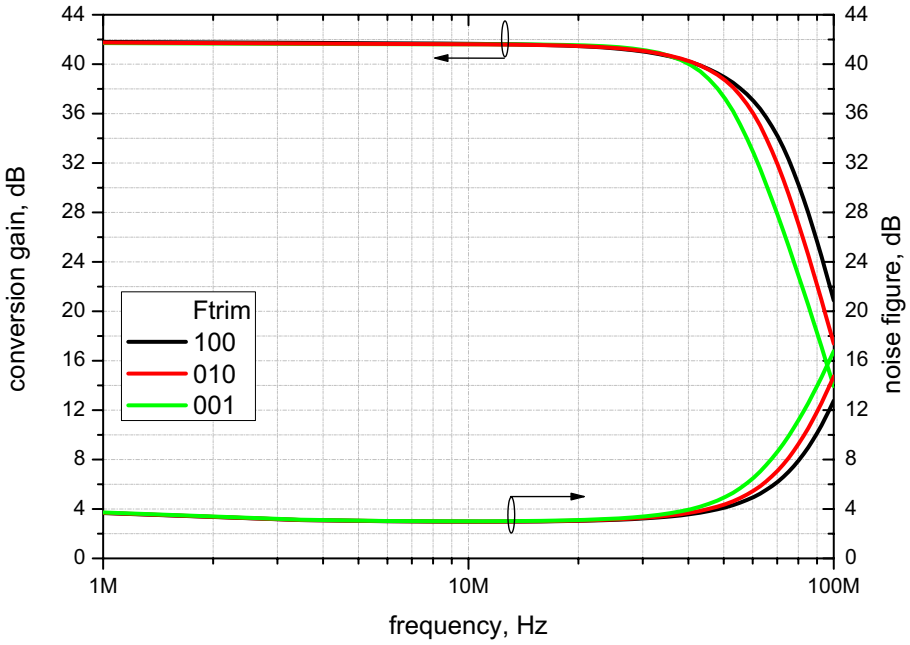


Figure 5.31: Corner frequency fine tuning.

Chip Layout

The designed chip layout is shown in Figure 5.34. The chip occupies the area of 1800 μm x 2000 μm. The positions of the building blocks are outlined with num-

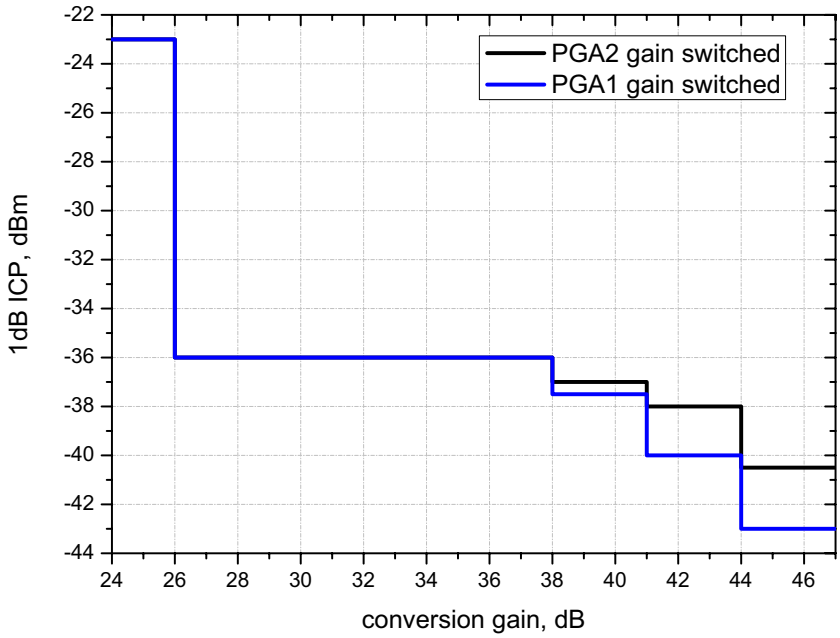


Figure 5.32: Simulated 1 dB ICP for different conversion gain settings.

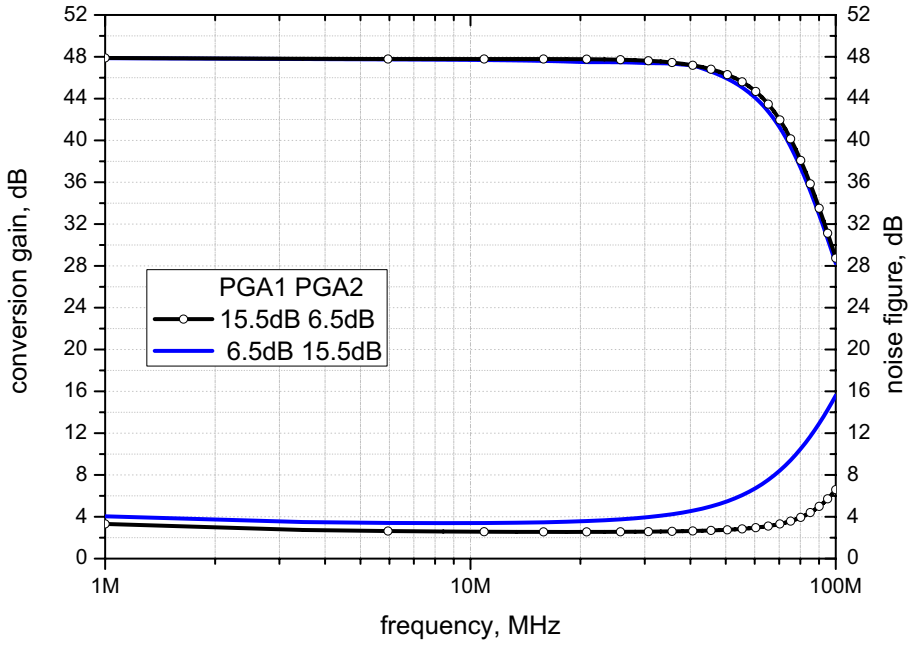


Figure 5.33: Simulated conversion gain and NF for different PGA settings.

bered black boxes and described in Table 5.3.

The layouting of the chip plays an important role on the final performance of

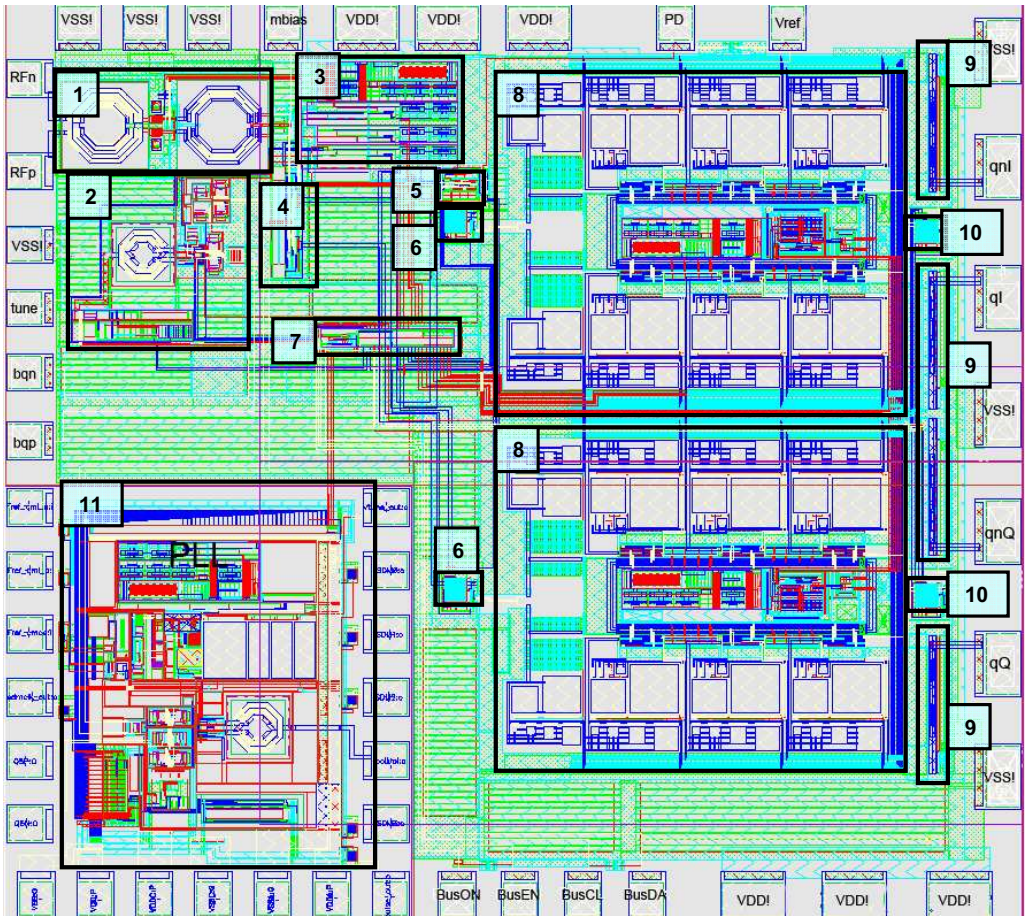


Figure 5.34: Layout of the implemented receiver.

Table 5.3: Block description.

Number	Desription
1	LNA
2	VCO and Divider
3	Biasing Circuit
4	Mixers
5	Power Detector and Comparator
6	PGA1
7	III Wire Bus Controller
8	BB Filter
9	Output Buffer
10	PGA2

the RF circuits. In order to minimize the parasitic effect which may influence the performance of the receiver the following issues were considered regarding the

floor planing and routing of the interconnections:

- Due to the differential structure, each block as well as the interconnections in between have to be as symmetrical as possible.
- All high frequency interconnections are realized in the top metalization layers to reduce parasitic capacitance to ground. Additionally, their series resistance is minimized due to a thicker metalization.
- The building blocks are arranged in that way that the length of the interconnections is minimized.
- Multiple ground pads, located around the die, and large ground plane on-chip ensure low impedance and homogeneous grounding of the chip.
- Large on-chip capacitors are implemented between the DC lines and ground to minimized the noise feed-through from the supply.

5.7 24 GHz Down-Converter

A simplified block diagram of the implemented down-converter is shown in Figure 5.35. The front-end consists of a differential tuned two-stage LNA, a double balanced mixer, a VCO, and an output buffer providing match to 50 Ω impedance of the antenna switch. According to the system frequency planning the down-

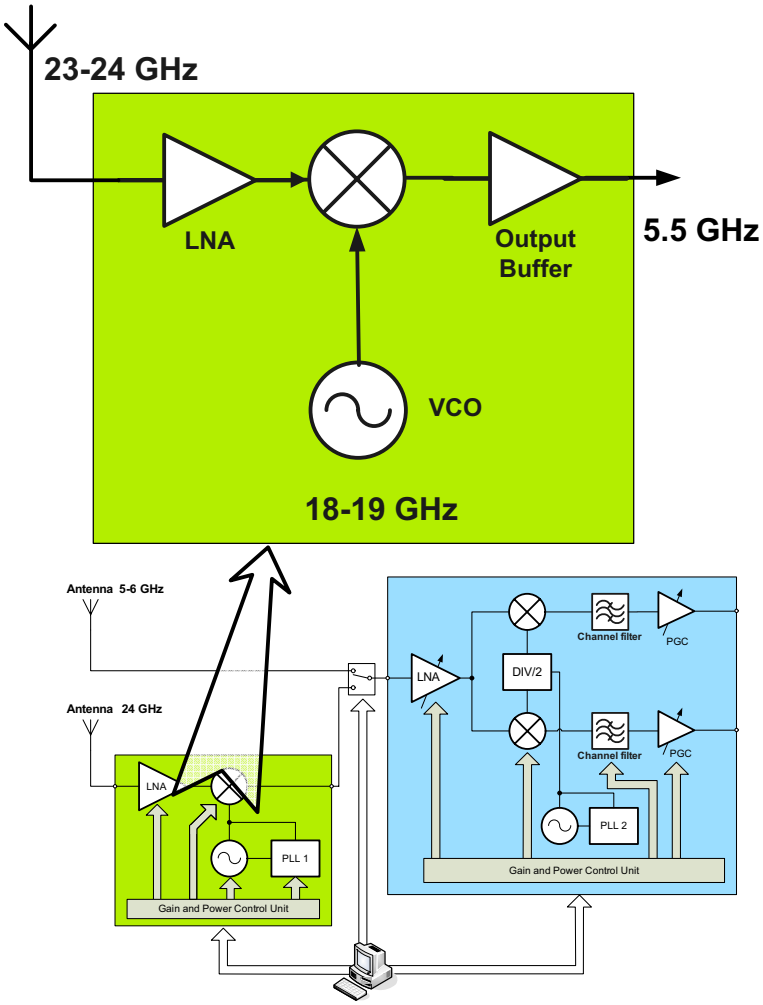


Figure 5.35: Block diagram of the down-converter.

converter should transform the input signal from 24 GHz range to the IF frequency of 5.5 GHz. Within this work no VCO were designed, therefore this circuit will not be mentioned in the further discussion.

Low Noise Amplifier

The chosen LNA topology is shown in Figure 5.36. The amplifier consists of two stages. The first stage is a differential common-gate structure. The second stage is a common-source used in order to enhance the overall gain of the receiver. The

supply voltage of the first stage is lowered by a transistor in a diode configuration. This enabled a direct coupling between the two stages. Both stages of the LNA work with tuned resonant circuits. Each of the resonant circuits consists of a center-tapped inductor and NMOS varactors. The inductors are implemented in the thick top metalization layer which minimizes the resistive loss and parasitic capacitance. Applying control signals to the nodes $dt1$ and $dt2$ tunes the LNA frequency characteristic between 23 and 24 GHz. The LNA drives 12.5 mA from a 1.5 V supply, from which 6.8 mA is consumed by the first stage and 5.7 mA is consumed by the second stage.

The common-gate structure does not suffer from significant Miller capacitance

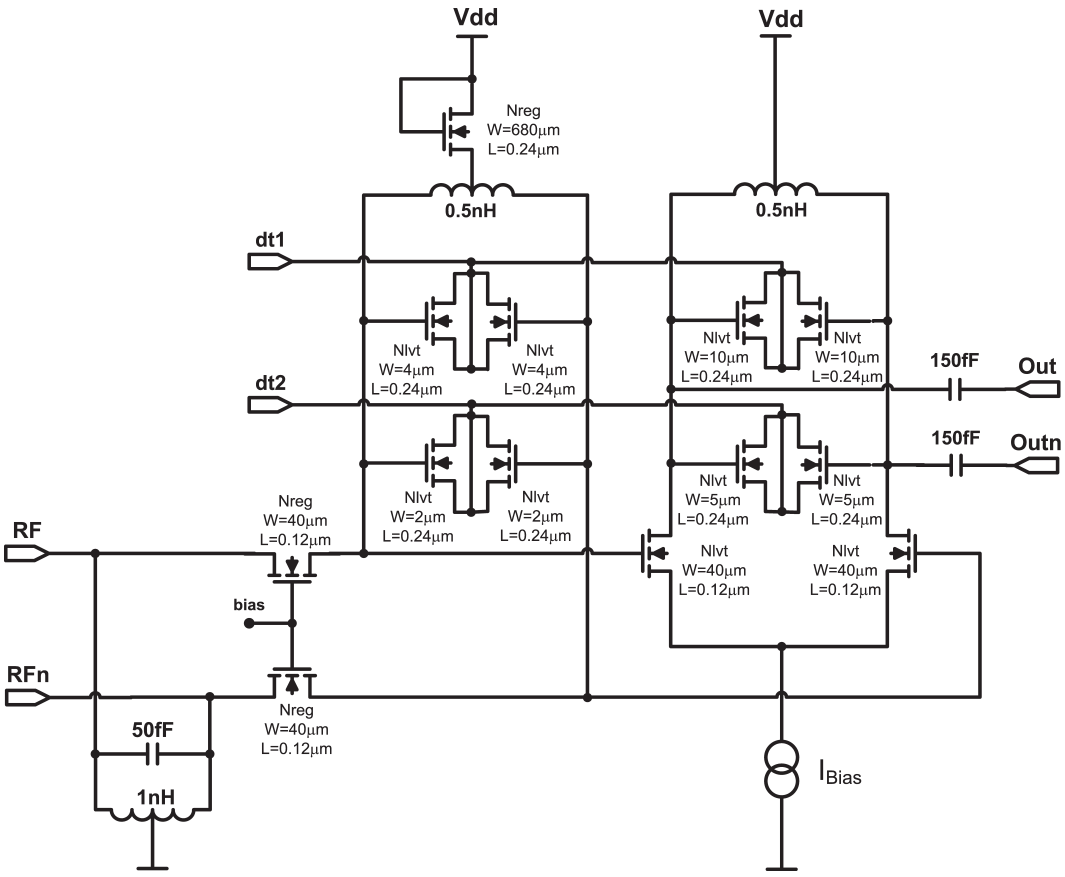


Figure 5.36: Schematic of a two stage LNA.

and the parasitic gate-source and gate-drain capacitances can be included in the input matching and load networks respectively. The center-tapped input inductor in parallel with capacitor and the parasitic capacitances of the input transistors form the input matching network. Additionally the input inductor provides a low impedance path to ground for DC and low-frequency signals so that the input matching network substitutes a lossy input ESD structure.

Down-Conversion Mixer

The schematic of the down-conversion mixer is shown in Figure 5.37. The mixer core is a double balanced Gilbert cell with a tuned load realized by a center-taped inductor and NMOS varactors. Such a solution helps to compensate technology and simulation (model inaccuracy) deviations in the frequency response of the mixer. The quality factor of the load inductor was kept at moderate level in order to obtain a broadband characteristic of the mixer. The mixer consumes 5.1 mA from a 1.5 V supply.

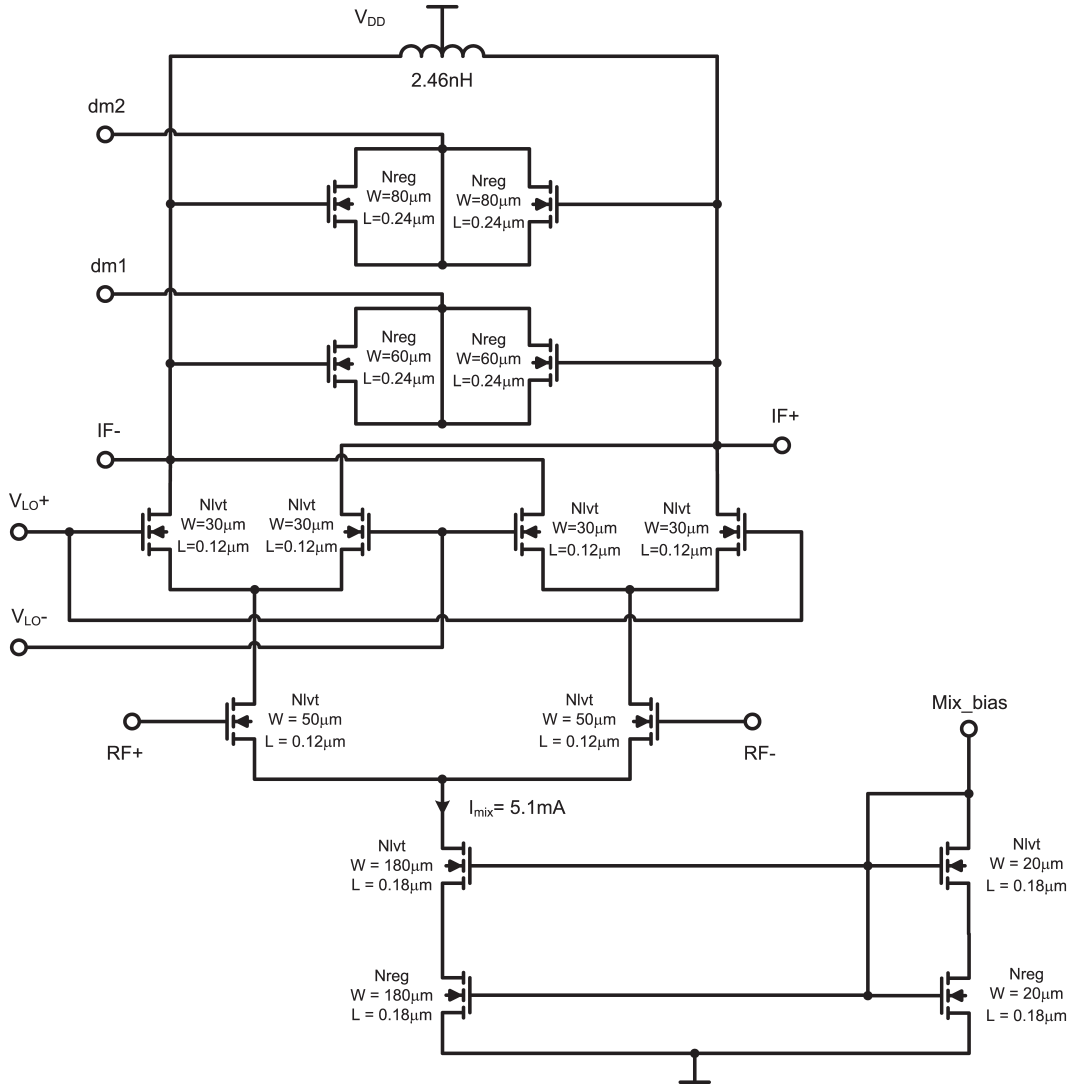


Figure 5.37: Schematic of a down-conversion mixer.

Simulated Performance of the Down-Converter

In order to achieve good accuracy, the inductor structures were simulated in electromagnetic simulator [Momentum 07], and then extracted S-parameters based

files were used to model the inductors.

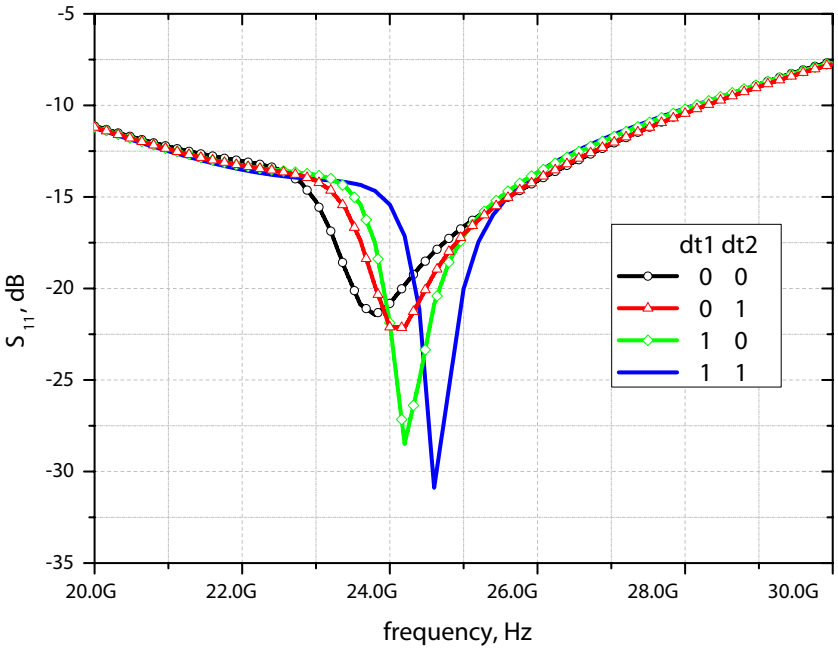


Figure 5.38: Simulated input insertion loss of the down-converter.

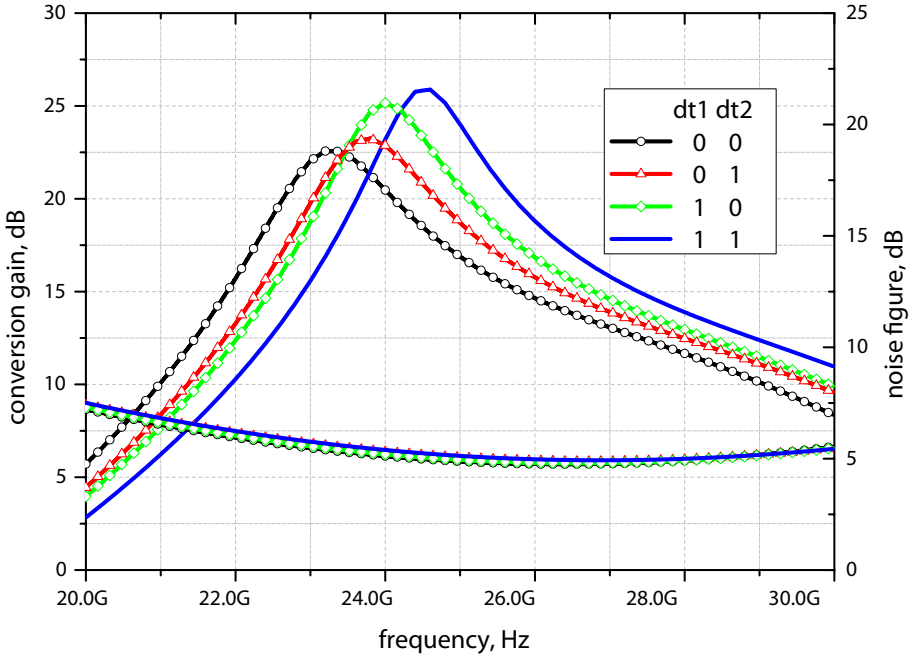


Figure 5.39: Simulated conversion gain and noise figure of the down-converter.

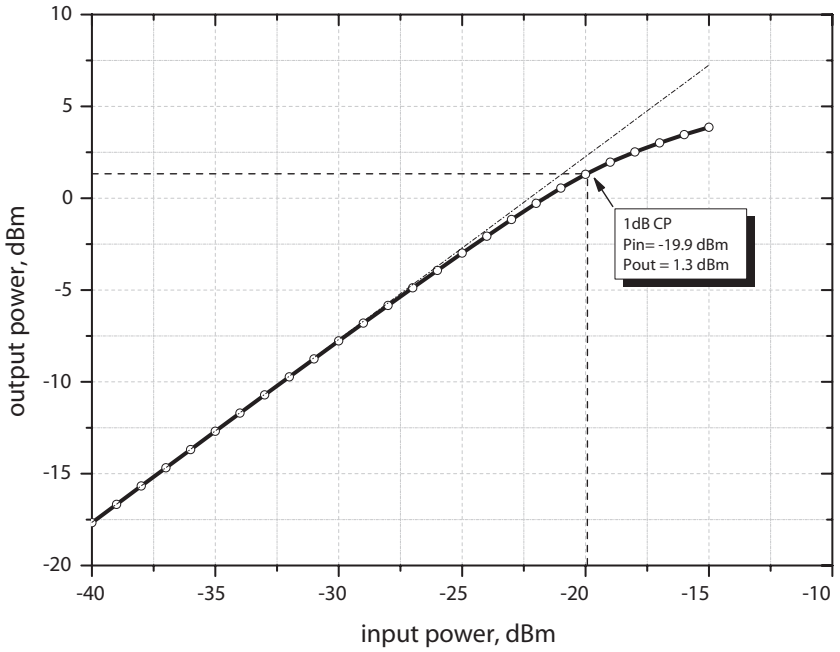


Figure 5.40: Simulated linearity of the down-converter at $RF_{in} = 24\,GHz$ and $IF = 5.5\,GHz$.

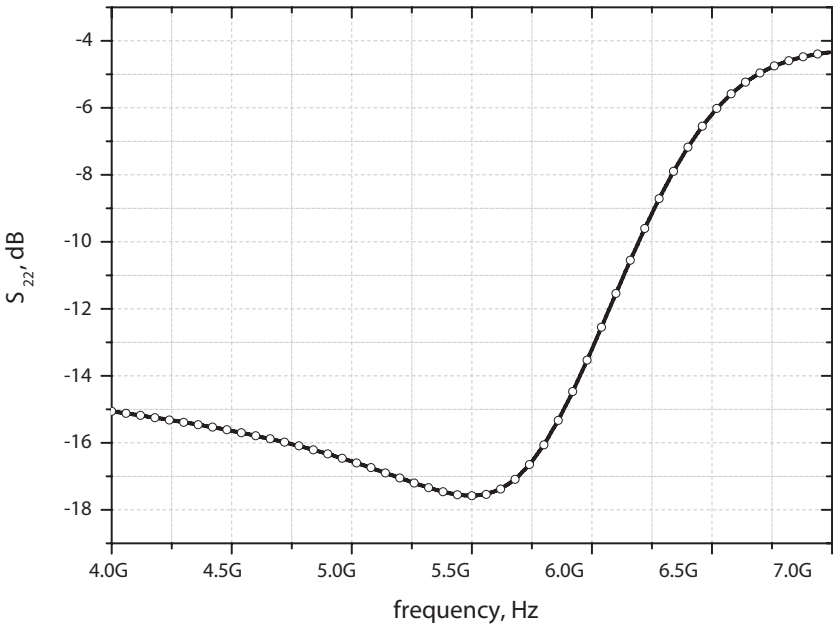


Figure 5.41: Simulated output insertion loss of the down-converter.

The simulated input insertion loss of the receiver is shown in Figure 5.38. Depending on the settings of the control inputs $dt1$ and $dt2$ the minimum of the trace is tuned, however, it remains below -15 dB for the frequency range of 23 - 24.5 GHz.

The conversion gain and the noise figure of the down-converter related to input signal frequency are shown in Figure 5.39. The overall gain exhibits more than 20 dB and the noise figure is below 6 dB in the frequency band of interest. The 1 dB ICP of the down-converter occurs at an input power of -19.9 dB as shown in Figure 5.40. The output insertion loss shown in Figure 5.41 does not exceed -15 dB in the range of 5 - 5.9 GHz providing good match to the 50 Ω output impedance. The performance of the 24 GHz down-converter is summarized in Table 5.4.

Table 5.4: The overall performance of the down-converter.

Parameter				
Peak Gain Frequency	23.2 GHz	23.8 GHz	24 GHz	24.6 GHz
Peak Power Gain	22.56 dB	23.25 dB	25.12 dB	25.85 dB
Noise Figure	5.40 dB	5.25 dB	5.20 dB	5.20 dB
Input Return Loss	-16.9 dB	-20.5 dB	-23.2 dB	-30.9 dB
Output Return Loss	< -15 dB			
1dB ICP	-19.9 dBm @ $RF_{in} = 24\,GHz$			
Power Consumption	40.3 mW @ $V_{DD} = 1.5\,V$			

The designed chip layout is shown in Figure 5.42. The chip occupies the area of 900 μm x 900 μm. Th positions of the building blocks are outlined with labeled black boxes. In order to minimize the parasitic capacitance to ground and the resistive losses all the high-frequency interconnections were routed in the top metalization layer. The input pads of the down-converter were doubled. This introduced extra shunt capacitance at the input of the LNA, however, it allows to minimize the inductance of the input bond-wires. The bon-wire inductance is difficult to predict since the bonding will be done by hand and has severe influence on the input matching. Therefore, it is worth to double the input pads which capacitance is easy to predict.

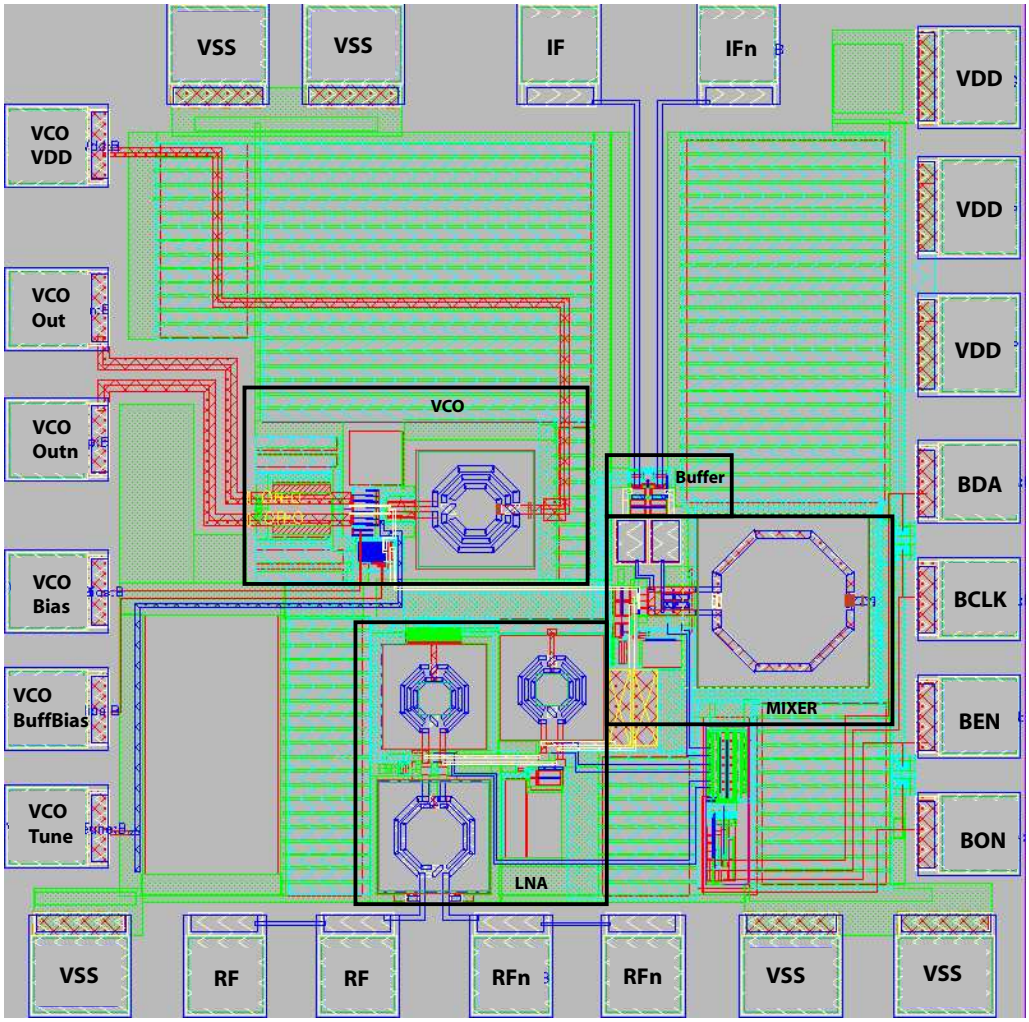


Figure 5.42: Layout of the implemented down-converter.

Chapter 6

Experimental Results

This chapter presents the measurement results of the implemented circuits. The receiver is a complex design, therefore, its most important building components have to be tested prior to combining them into a fully integrated solution. At first, a standalone common-gate LNA implemented to verify the capabilities of this structure will be presented [Debski 07,a]. In the next step, a down-converter utilizing the LNA, two mixers a VCO and a frequency divider is characterized. Finally, the measurement results of a fully integrated 5 - 6 GHz receiver with analog preprocessing and 24 GHz down-converter ([Debski 07,b]) are presented.

6.1 5-6 GHz Low-Power, High Linearity Differential CMOS LNA with Robust ESD Protection

The schematic diagram of a differential common-gate LNA with an output buffer is illustrated in Figure 6.1. Since the LNA is designed for a further integration in a WLAN receiver, the output buffer was used only for measurement purposes.

The transistors M1 work in common-gate configuration so that the RF input is connected to the source of the transistor instead of the gate, which prevents the input ESD from discharge through the thin gate oxide [Tang 04]. Additionally, the structure does not suffer from a significant Miller capacitance between input and output terminals and the parasitic gate-source and gate-drain capacitances can be absorbed by an input matching and a load network respectively. The center-tapped inductor L_{in}, together with the capacitor C_{in} and parasitic gate-source capacitances form the input matching network. The on-chip center-tapped input inductor (L_{in}=2 nH, with parasitic series resistance of 1.1 Ω) provides a low impedance path to ground for DC and low frequency signals, preventing the input transistors from damage during ESD stress. The load tank of the amplifier consists of a center-tapped inductor L_{load} with parallel connected NMOS varactors

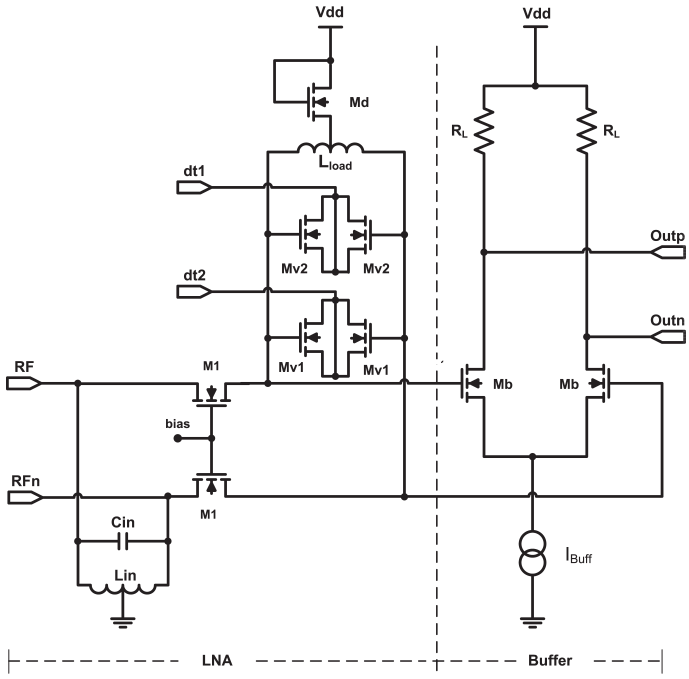


Figure 6.1: Schematic of a common-gate LNA with an output buffer.

(Mv1, Mv2). Applying digital signals to NMOS varactors (pins dt1, dt2) the center frequency of a narrow-band LNA characteristic can be tuned, achieving an overall 3 dB bandwidth of 1 GHz. Such a tuning technique allows utilizing the advantages of a narrow-band amplifier with wide frequency coverage. The transistor Md lowers the supply voltage of the LNA form 1.5 V down to 0.9 V which makes the LNA feasible to be DC coupled to the following stages working with a 1.5 V supply voltage. The output buffer is a differential common source amplifier with a resistive load. It delivers a high impedance termination (similar to a mixer) for the LNA and is capable of driving a 50 Ω load impedance.

The LNA chip which occupies an area of 450 μm x 900 μm was mounted on a Rogers RO4003 substrate. Aluminum bond-wires connect the chip with the test board as shown in Figure 6.2. The influence of the bond-wires has been taken into account during the simulation process.

The gain and noise performance of the LNA is shown in Figure 6.3. The LNA consumes a DC power of 7.5 mW and exhibits 16.5 dB gain and 2.9 dB noise figure at 5.5 GHz. The overall 3 dB bandwidth of 1GHz is achieved by switching NMOS varactors in the load of the LNA. The measured input and output reflection coefficients are shown in Figure 6.4. The measured gain compression and two tone test results are presented in Figure 6.5. The input P_{1dB} is -6.5 dBm and the input IP3 is 4.2 dBm at 5.5 GHz. Additionally, to prove the ESD robustness of the circuit, HBM pulses of ± 2 kV were applied to the input of the common-gate LNA causing no change to its performance.

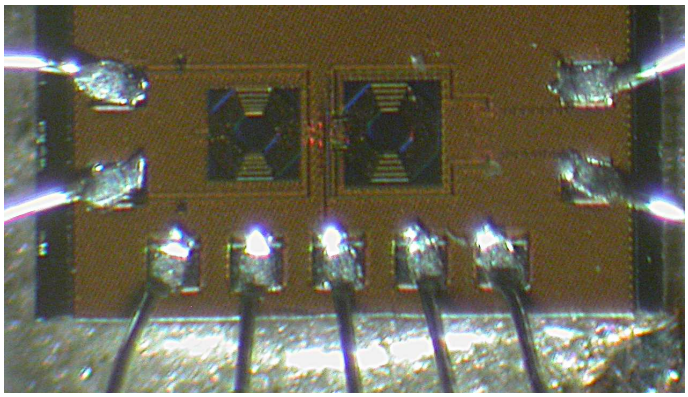


Figure 6.2: Die photograph of the fabricated amplifier.

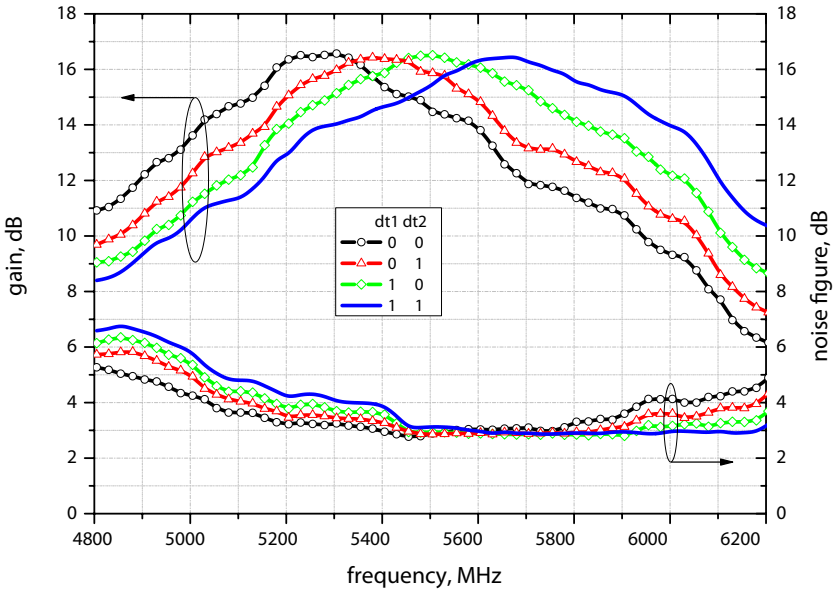


Figure 6.3: Measured gain and noise figure.

A figure of merit (FOM) introduced in [Chandrasekha 02] is used in order to compare this work with recently published LNAs. This FOM takes into account the gain, the noise figure, the linearity, the power consumption and the frequency of operation of the amplifier. It is given as

$$FOM = 10\log\left(100\left(\frac{|S_{21}|(linear)f_0^2}{(F-1)P_{dc}(mW)}\right)\left(\frac{IOP3(mW)}{P_{dc}(mW)}\right)\right) \tag{6.1}$$

where f_0 is the operating frequency normalized to 1 GHz and F is the noise figure. The comparison of the recently published LNAs with this work is shown in Table 6.1. The presented LNA outperforms all other LNAs, indicating the suitability of the presented structure for modern commercial wireless applications.

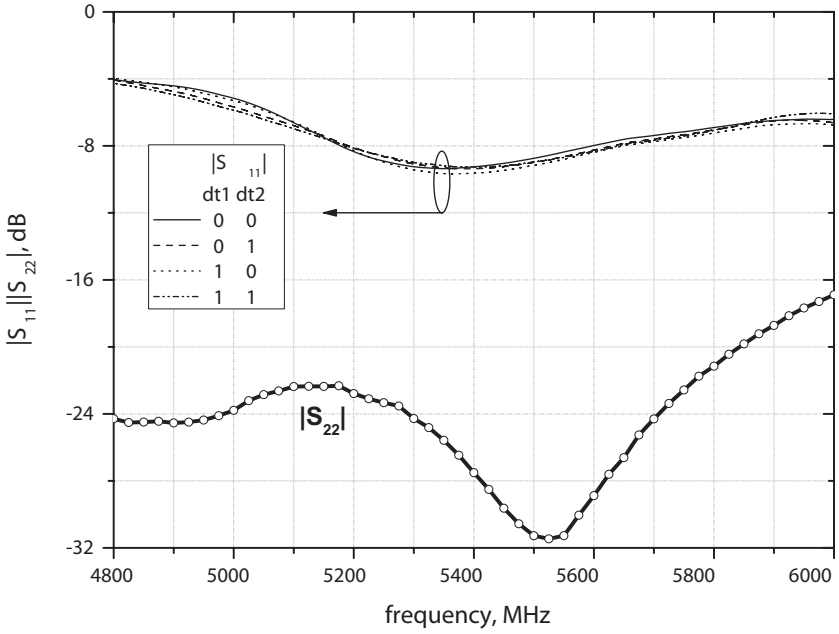


Figure 6.4: Measured input and output insertion losses.

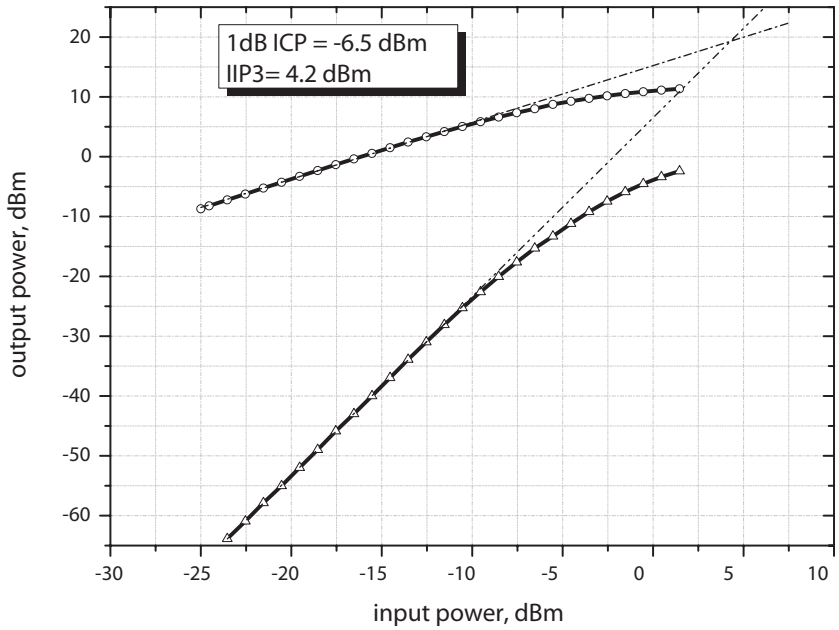


Figure 6.5: Measured 1 dB ICP and IP3.

6.2 5 - 6 GHz Zero-IF Down-Converter

Having characterized the performance of the common-gate LNA, a down-converter chip shown in Figure 6.6 has been designed. The circuit consists of a LNA, two

Table 6.1: Performance Comparison of recently published LNAs.

Ref.	Freq [GHz]	NF [dB]	S21 [dB]	IIP3 [dBm]	Pdc [mW]	FOM
[Gramegna 01]	0.90	1.00	13.00	-1.5	8.55	24.31
[Chandrasekha 02]	2.4	2.77	12.10	2.40	4.65	35.30
[Leroux 02]	1.57	1.30	16.50	-5.0	9.00	27.66
[Linten 05]	5.00	2.90	13.45	-2.7	9.72	32.00
[Tang 04]	1.80	5.00	14.10	-7.6	30.00	5.56
This work	**5.50**	**2.90**	**16.50**	**4.27**	**7.50**	**45.06**

down-conversion mixers, a VCO and a frequency divider. The schematic of the

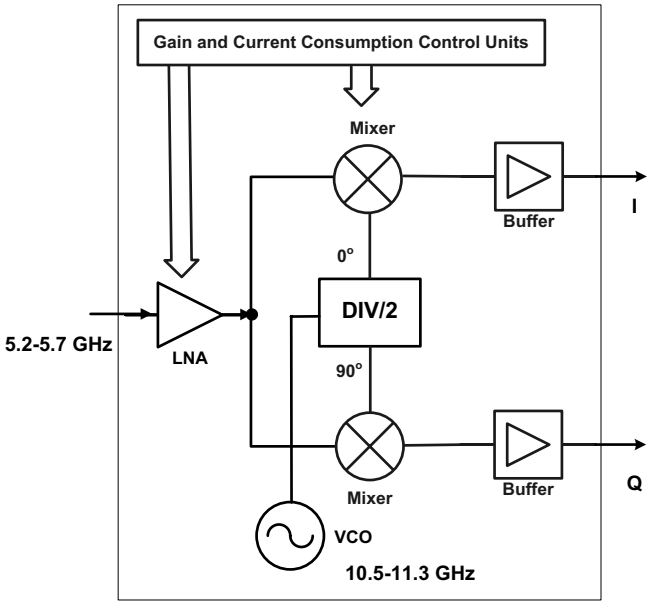


Figure 6.6: Block diagram of the implemented down-converter.

LNA is shown in Figure 6.7. It utilizes a common-gate amplifier structure with digitally tuned frequency characteristic which was tested in the first design step. The input matching network parameters were optimized to provide an input return loss lower than -10 dB for all tuning settings. The schematic of the implemented mixer is shown in Figure 6.8. The mixer core is a double balanced Gilbert cell with PMOS transistors used as load in order to lower the flicker noise [Binkley 02]. The LO signal is fed to the divider to provide the phase shift for quadrature demodulation. The output buffers, capable of driving 50 Ω termination impedance, are implemented for measurement purposes.

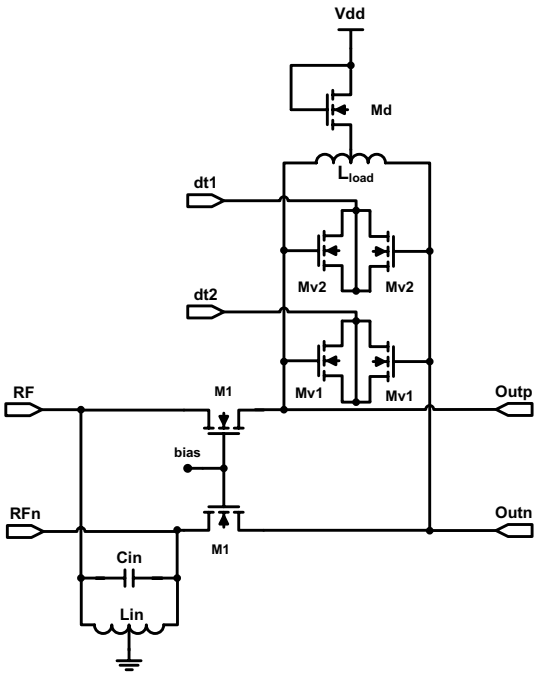


Figure 6.7: Schematic of the common-gate LNA.

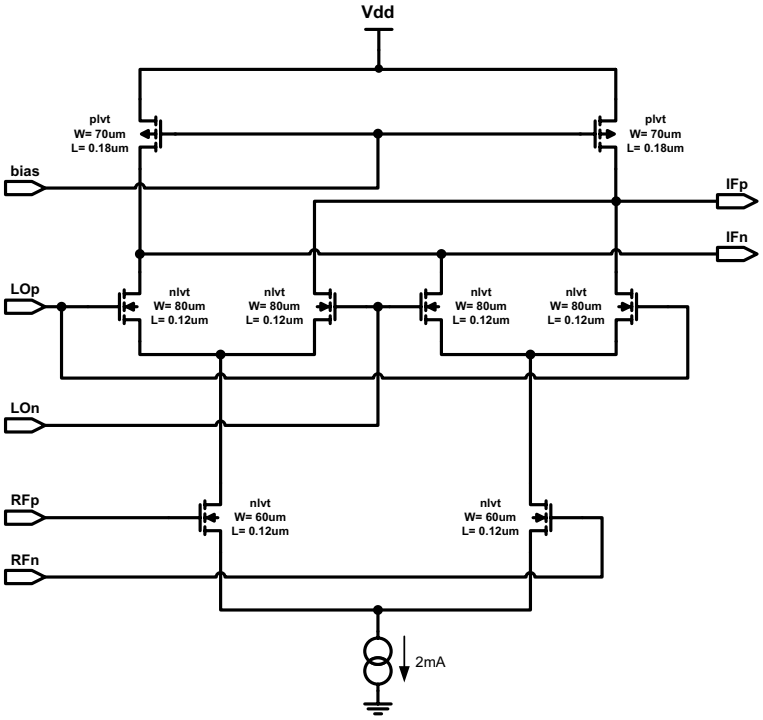


Figure 6.8: Schematic of the down-conversion mixer.

The fabricated chip was mounted on a Rogers RO4003 test board, as shown in Figure 6.9. The chip was glued in the middle of the board using conductive glue. The terminals of the IC are wire-bonded with aluminum bondwires. All high fre-

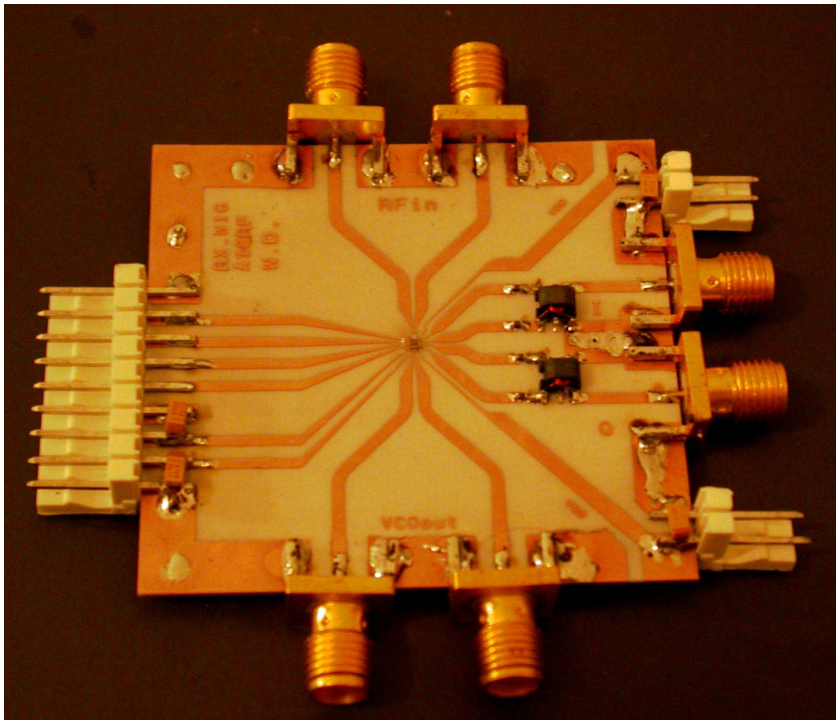


Figure 6.9: Down-converter test board.

quency signals are guided with 50 Ω microstrip lines to SMA connectors which are soldered at the edge of the test board. SMD hybrids are mounted to convert differential I and Q outputs to single-ended form to ease the measurements. In order to minimize voltage ripples and to prevent oscillation, all DC lines are blocked by a 10 pF and a 0.1 μF SMD capacitors.
The measurements of the input return loss are presented in Figure 6.10. The influence of the SMA connectors and feeding lines were de-embedded. Therefore the measurements present the performance of the chip with bondwires. The characteristic of the input return loss is tuned depending on the LNA settings. The circuit shows good input match to 50 Ω input impedance for all the tuning settings. The frequency response and noise figure measurements of the down-converter are shown in Figure 6.11. The circuit exhibits a conversion gain of 24.5 dB and a noise figure of 3.7 dB at the output frequency of 25 MHz. The overall frequency band of operation of the down-converter was limited by the tuning range of the VCO to 5.15 - 5.7 GHz. In this frequency range the noise and gain performance was the same as presented in Figure 6.11. Finally, linearity measurements were performed for the investigated circuit at an IF frequency of 25 MHz. By sweeping the power of the input RF signal, the 1 dB compression point is extracted from the measured

baseband output signal. The linearity measurement is shown in Figure 6.12.

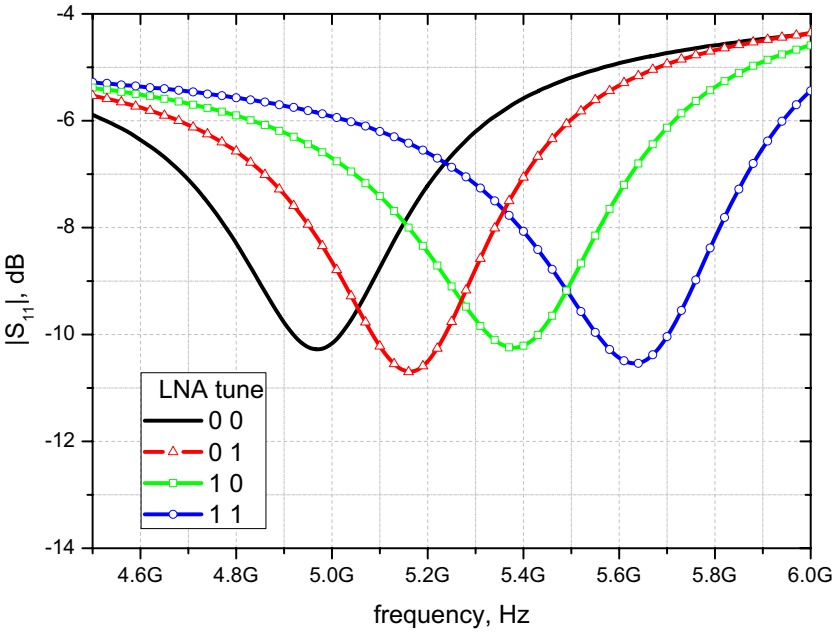


Figure 6.10: Measured insertion loss of the down-converter.

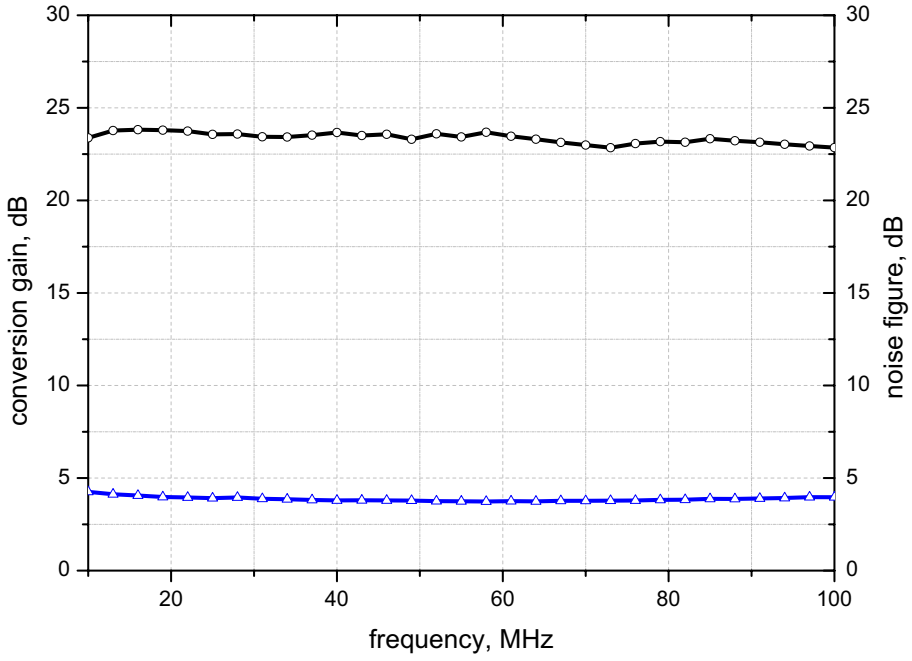


Figure 6.11: Measured conversion gain and noise figure of the down-converter.

The measurement results of the down-converter are summarized in Table 6.2.

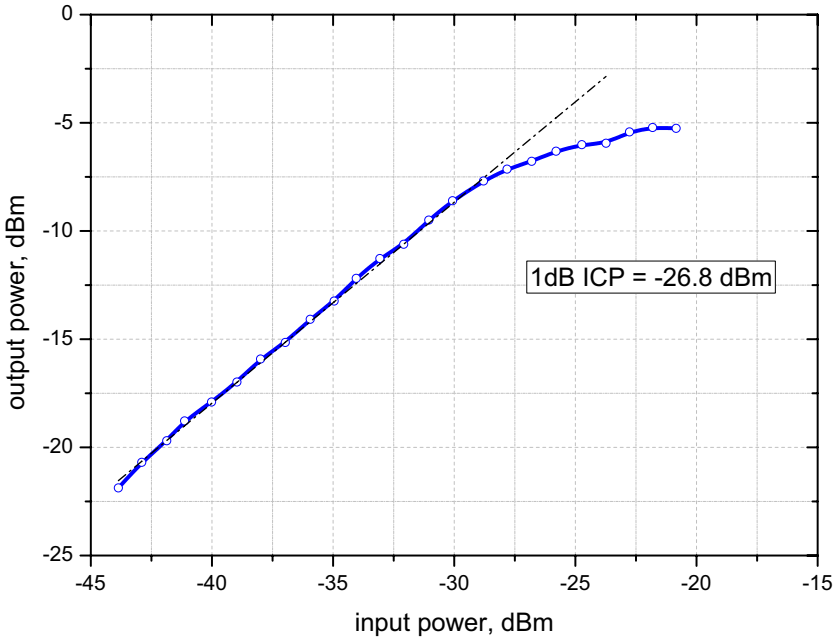


Figure 6.12: Measured linearity of the down-converter.

Table 6.2: The overall performance of the receiver.

Bandwidth	5.15 - 5.7 GHz
Overall Gain @ 25 MHz	24.5 dB
Noise Figure @ 25MHz	3.7 dB
Overall 1 dB ICP	-26.8 dBm
S_{11}	< -10 dB
Power Consumption	49.5 mW @ $V_{DD} = 1.5\,V$

Demonstrator board

Having characterized the performance of the RF front-end and the channel select filter (performed by other colleagues from our team) a demonstrator board shown in Figure 6.13 was developed. The board includes the RF front-end chip, two channel select filters and a frequency divider in order to feed in the LO signal to a commercial PLL. A microstrip rat-race hybrid was designed to provide a differential input signal to the down-converter chip from a single-ended signal source. Three SMD voltage down-regulators are used in order to provide proper biasing for each IC from a single 5 V supply.

The measured frequency response and noise figure of the circuit are shown in Figure 6.14. The receiver exhibits a conversion gain of 40.5 dB and a noise figure of 7.5 dB at the IF of 25 MHz. It can be noticed that the noise figure starts to grow at low frequencies and reaches the value of 10 dB at the IF of 1 MHz. This proves

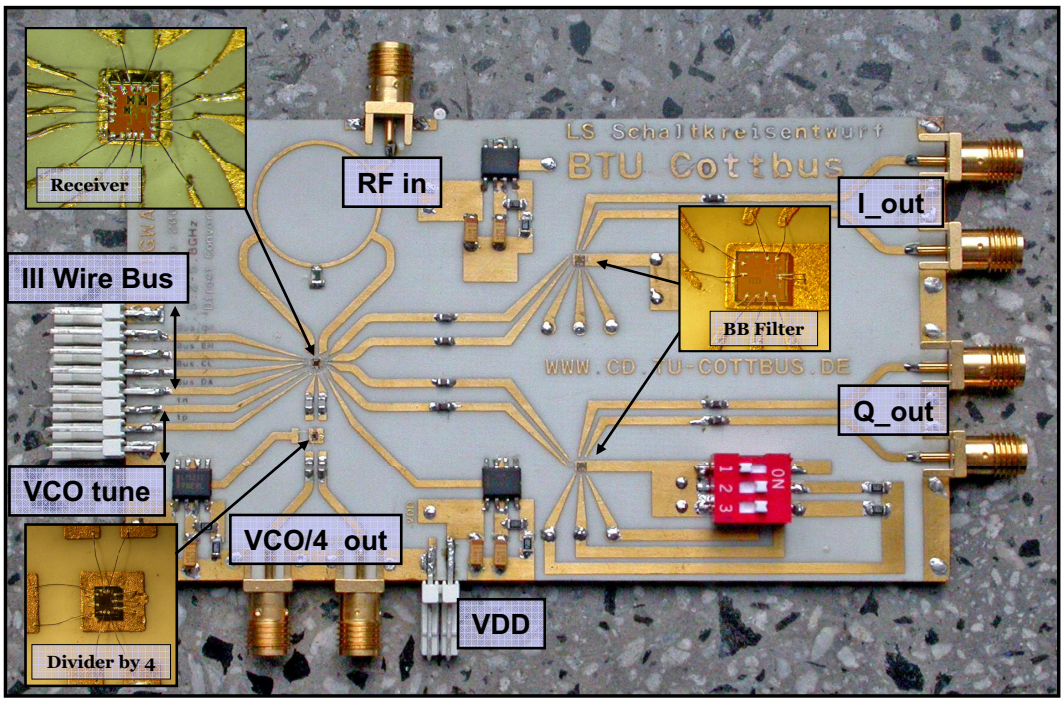


Figure 6.13: Photograph of the demonstrator board.

a strong degrading filter contribution to the flicker noise. Finally, the linearity of the circuit was investigated. The measurement results in Figure 6.15 show that the 1 dB input compression point is reached at the input power of -44 dBm.
The measurement results of the demonstrator board show the strong contribution of the noise figure of the filter to the overall performance. The achieved noise figure of 7.5 dB is much higher than specified by the system requirements. The overall linearity has to be improved to enable the receiver to operate in a WLAN environment. One of the possible ways to minimize the noise contribution of the filter is to increase the gain in the RF front-end, however the linearity has to be kept on the required level. Those conclusions led us to the final system architecture and circuit level implementations. The gain of the building blocks was distributed in the way that the noise figure defined by the system requirements is achieved while providing sufficient linearity to cope with high input signal levels.

6.3 5 - 6 GHz Zero-IF Receiver with Analog Pre-Processing

In order to characterize the receiver, the fabricated chip was mounted on a Rogers RO4003 test board. The IC is attached to the board using a conductive glue and its terminals are wire-bonded to the board with aluminum bondwires (diame-

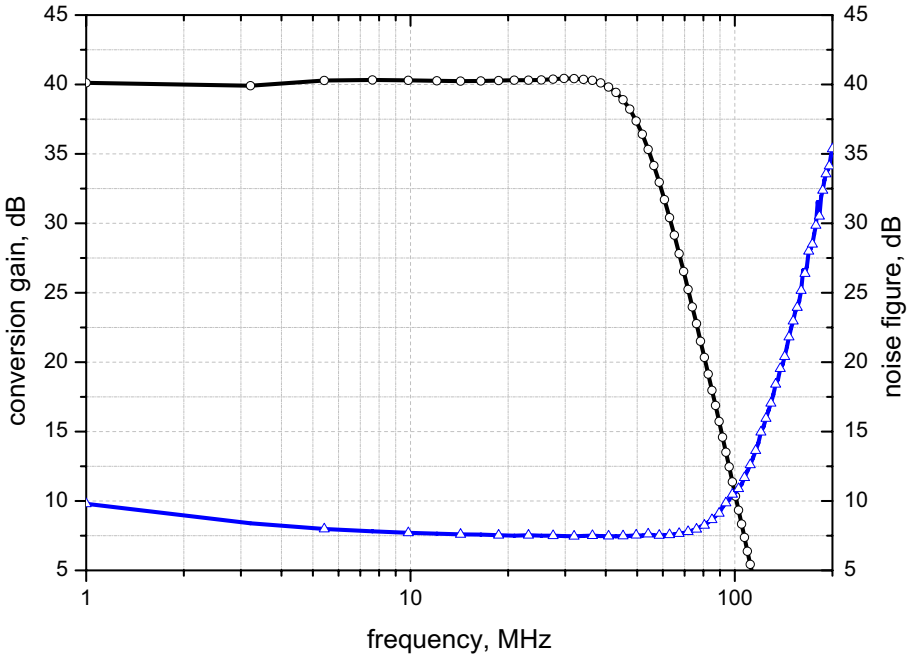


Figure 6.14: Conversion gain and noise figure of the down-converter and channel-select filter.

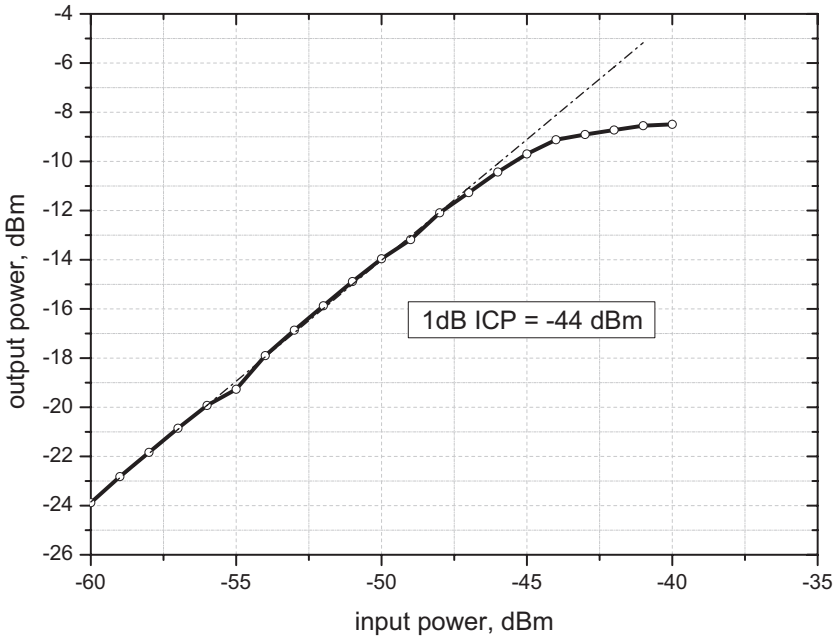


Figure 6.15: Linearity of the down-converter and channel-select filter.

ter = 25 μm), as shown in Figure 6.16. On board, the RF signals are guided with transmission lines with a characteristic impedance of 50 Ω. At the end of each mi-

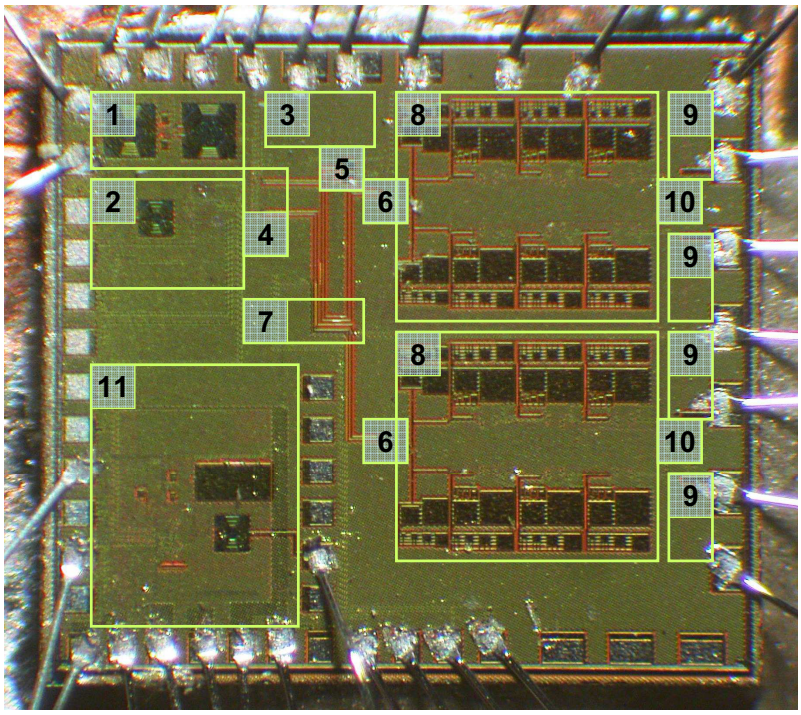


Figure 6.16: Photograph of the bonded receiver chip.

Table 6.3: Block description.

Number	Desription	Number	Desription
1	LNA	2	VCO and Divider
3	Biasing Circuit	4	Mixers
5	Power Detector and Comparator	6	PGA1
7	III Wire Bus Controller	8	BB Filter
9	Output Buffer	10	PGA2

crostrip line SMA connectors are mounted. Additionally, to provide single-ended outputs, SMD hybrids convert differential I and Q outputs to single-ended. All on-chip grounds are connected to the common ground on the PCB with multiple bondwires. In order to minimize voltage ripples and to prevent oscillations all DC lines are blocked by a 10 pF and a 0.1 μF SMD capacitor. To guarantee mechanical stability and good ground connection, the board is mounted on a aluminum block. Figure 6.17 shows a photograph of the test fixture.

Input Return Loss Measurement

The measurements of input reflection coefficient are presented in Figure 6.18. The influence of the SMA connectors and feeding lines has been de-embedded, thus, the results present the input return loss of the chip with bondwires. Depending on the LNA setting, the characteristic of the input return loss is tuned in frequency.

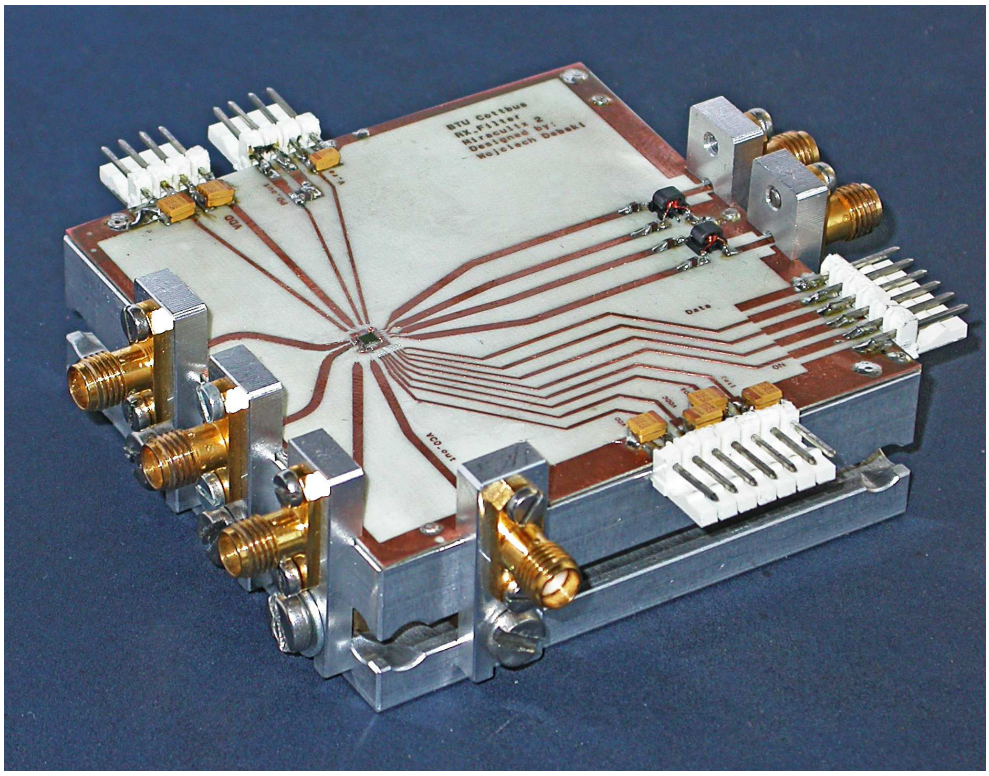
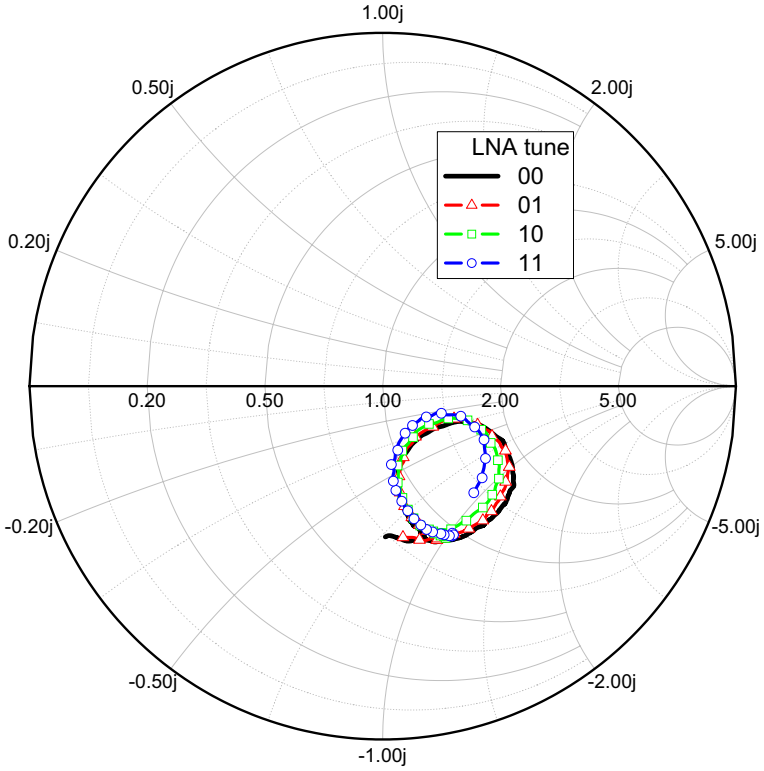
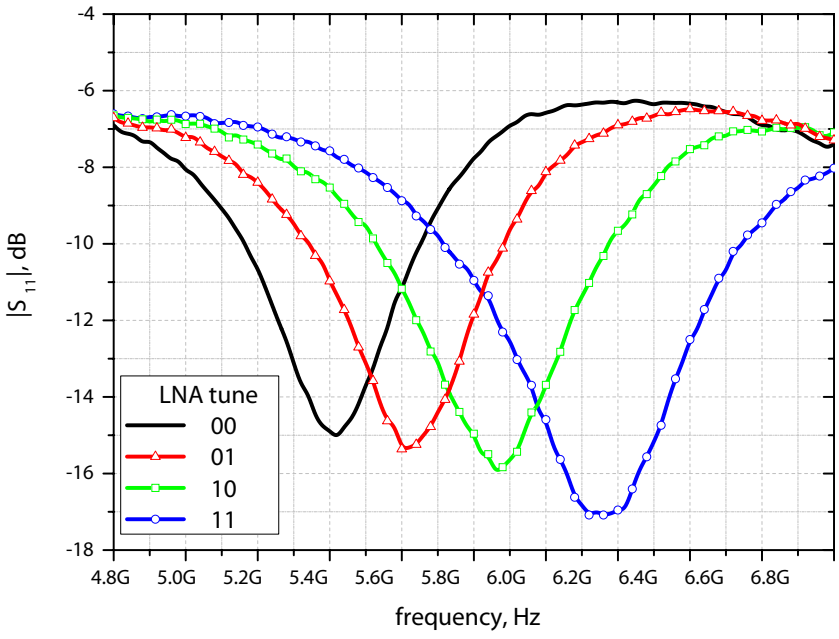


Figure 6.17: Receiver test fixture.

It can be noticed that the characteristic is shifted a bit to higher frequencies, however, the commonly accepted specification of -10 dB input reflection is met over the frequency range of 5.15 - 6 GHz, covering all available WLAN bands in this range.



(a)



(b)

Figure 6.18: Measured insertion loss of the receiver.

Frequency Response and Noise Figure of the Receiver

In order to fully characterize the frequency response and the noise figure of the receiver, three sets of measurements were carried out. First, the cutoff frequency of the filter was set to 50 MHz and the conversion gain and the noise figure was performed for all gain settings of the first PGA. This is the case when the receiver will operate at the best noise performance which will be the case for input signals close to the noise floor. The measurement results are shown in Figure 6.19. The receiver exhibits the overall noise figure of 3.8 dB at 43.4 dB of conversion gain. As the gain is reduced, the noise figure raises to 6.3 dB at the conversion gain of 33.5 dB. This phenomenon proves the destructive influence of the filter noise on the overall noise performance of the receiver. Those measurements were performed for the input signal frequencies set to 5.2 GHz, 5.4 GHz, 5.6 GHz and 5.9 GHz. The obtained conversion gain and noise figure deviate maximally by 2 dB and 0.15 dB from the ones presented in Figure 6.19, respectively.

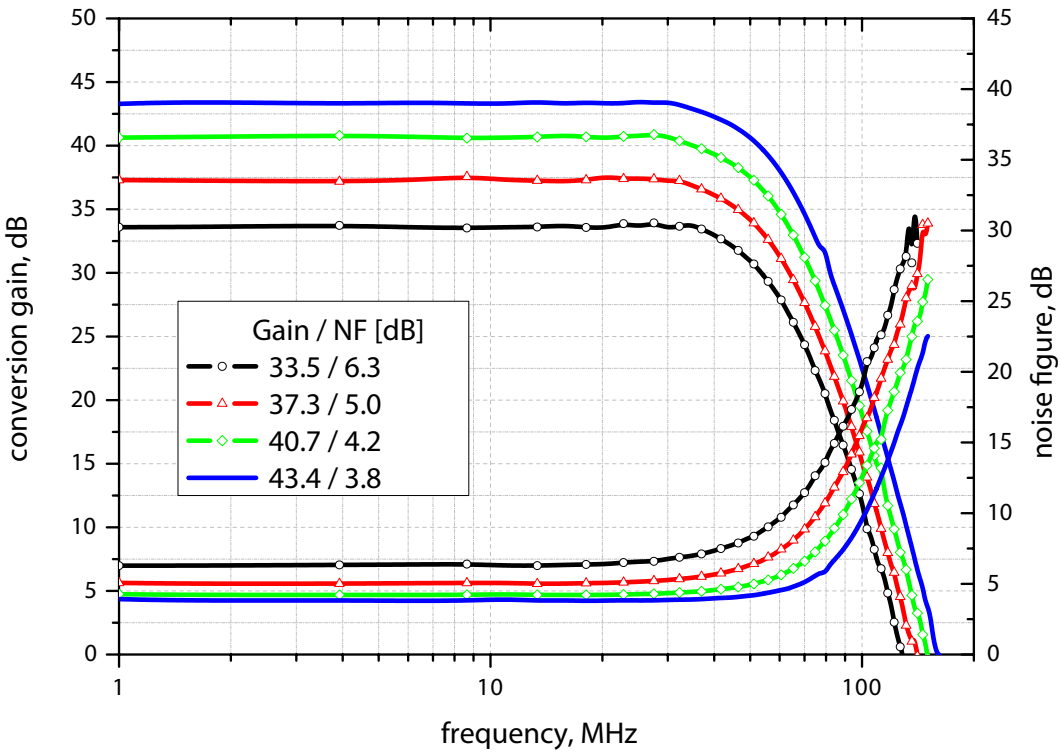


Figure 6.19: Measured conversion gain and noise figure for different PGA settings.

The measurement results presented in Figure 6.20 show the conversion gain and the noise figure for different cutoff frequencies of the filter. The cutoff frequency of the implemented filter can be digitally adjusted to 6.5 MHz, 10 MHz, 20 MHz 50 MHz which corresponds to the required values specified by system requirements. Additionally, each of the corner frequency can be fine-tuned by means

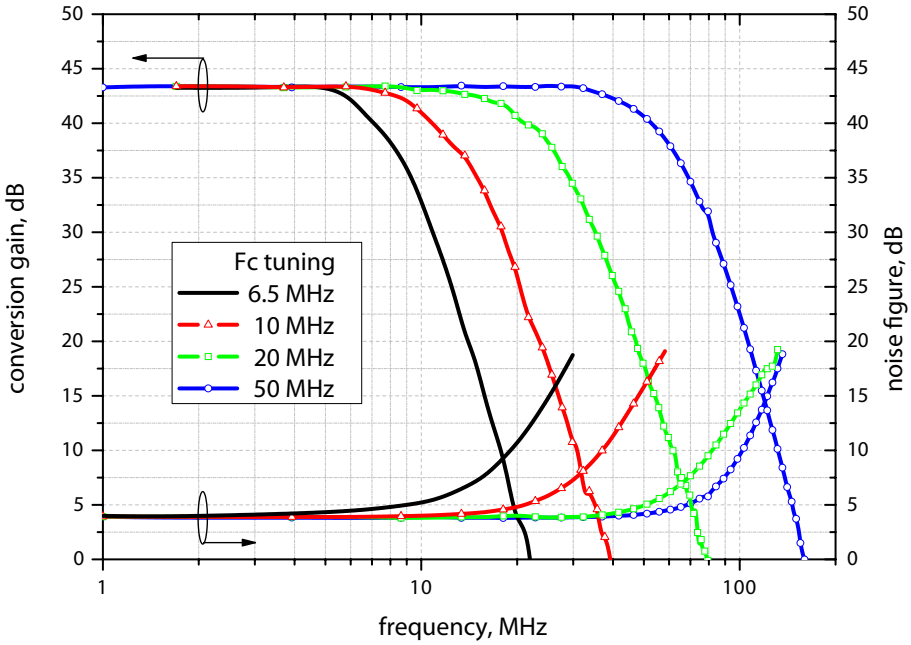


Figure 6.20: Measured conversion gain and noise figure for all obtainable cutoff frequencies.

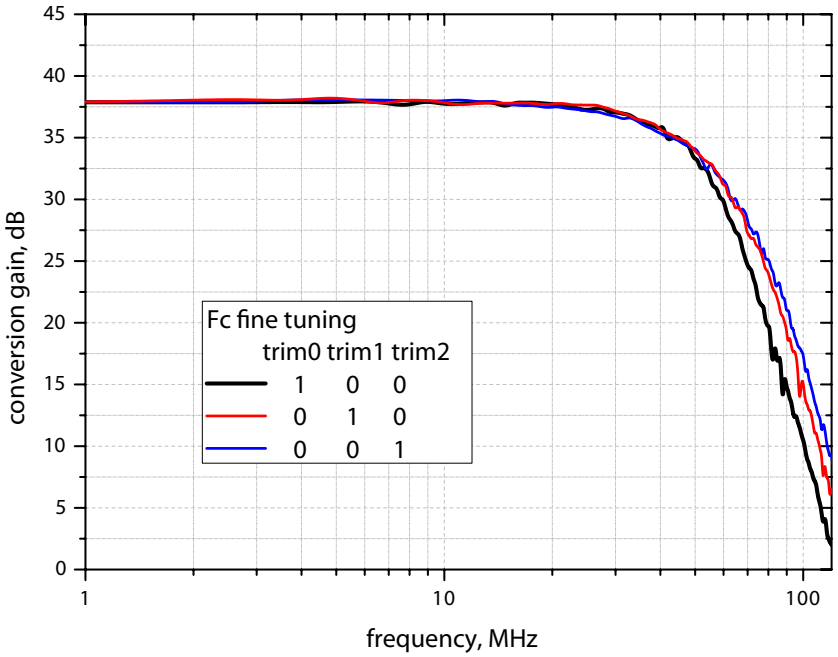


Figure 6.21: Fine tuning of the cutoff frequency of the BB filter.

of three bits: $trim0$, $trim1$ and $trim2$. The fine-tuning of the cutoff frequency presented in Figure 6.21 can be used to compensate the component parameter

deviations and performance spread of the fabricated chips.

Linearity Measurement

The linearity measurements of the receiver were performed for the RF input signal of 5.2 GHz and the IF of 25 MHz. By sweeping the power of the signal source, the 1dB compression point is extracted from the measured baseband output signal. The measurements were performed for all achievable conversion gains of the receiver. The results shown in Figure 6.22 present the linearity of the receiver for the case when only one of the PGAs is switched and the other one is bypassed. It is obvious that the best linearity is achieved when the second amplifier works and the first one is bypassed. The achieved performance meets the requirements for the 5 GHz WLAN band.

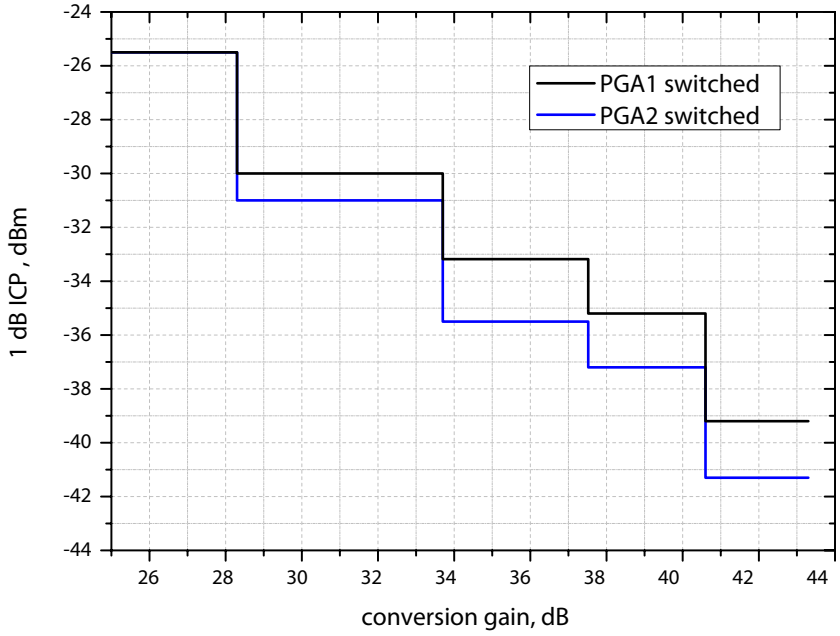


Figure 6.22: Measured 1 dB ICP versus conversion gain of the receiver.

Power Detector Characterization

In order to characterize the power detector, the IF signal was set to 50 MHz which corresponds to the adjacent channel. By sweeping the power of the input signal, the changes in the output voltage of the power detector were measured. The resultant characteristic of the power detector is shown in Figure 6.23.

It is also interesting to investigate what is the delay between the appearance of

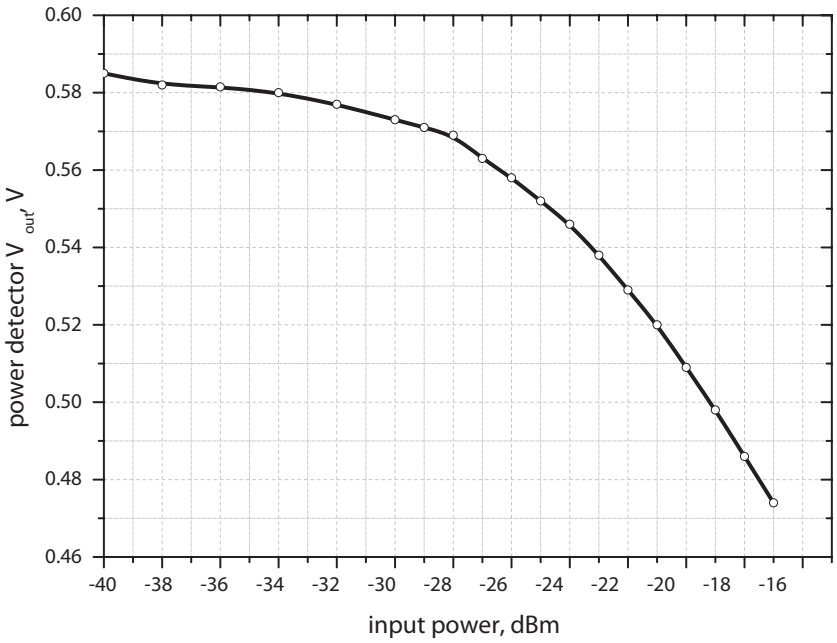


Figure 6.23: Measured power detector response.

a blocker signal at the receiver input and the response of the power detector. In order to investigate such case, a test circuit shown in Figure 6.24 was built. The

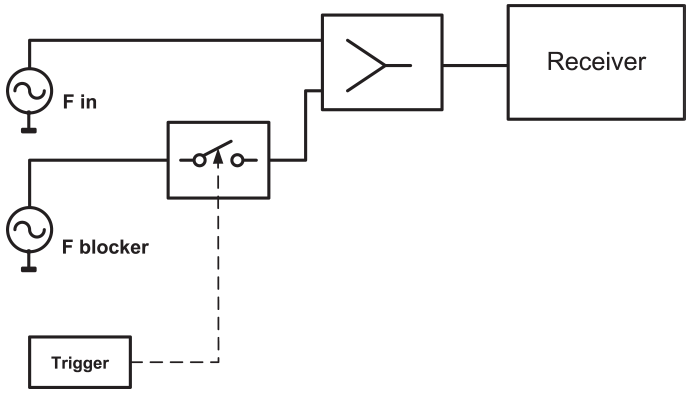


Figure 6.24: Test setup for the characterization of the power detector time response.

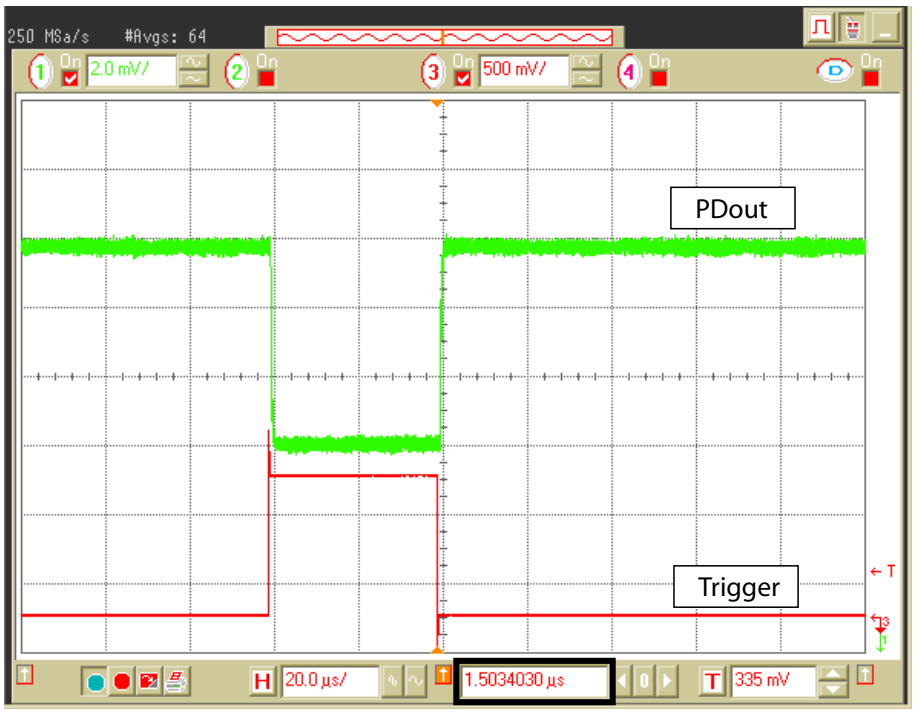


Figure 6.25: Power detector time response.

test setup includes two signal generators, a power combiner and an oscilloscope. One of the signal generators supplies an interferer which is combined with the wanted signal and both are fed into the receiver input. The interferer signal is triggered by the oscilloscope which monitors the output of the power detector. The measured time response of the power detector is shown in Figure 6.25. The measured delay between the appearance of the interferer and the response of the power detector is 1.5 μs.

Receiver Performance Summary

The performance of the characterized receiver is summarized in Table 6.4.

Table 6.4: The overall performance of the receiver.

Bandwidth	5.1 - 6 GHz				
Overall Gain @ 25 MHz	25.5 dB	33.5 dB	37.3 dB	40.7 dB	43.4 dB
Noise Figure @ 25MHz		6.3 dB	5.0 dB	4.2 dB	3.8 dB
Overall 1 dB ICP	-25.5 dBm	-30 dBm	-33.2 dBm	-35.2 dBm	-39.2 dBm
S_{11}	$<$ -10 dB				
Power Consumption	140 mW @ $V_{DD} = 1.5\,V$				

A comparison of the measured receiver performance with simulation results is shown in the following figures. As depicted in Figure 6.26, the input insertion loss

characteristics is shifted to higher frequencies which may be caused by smaller real parasitics than expected. However, despite the shift the insertion loss does not exceed the level of -10 dB in the desired frequency range. The conversion

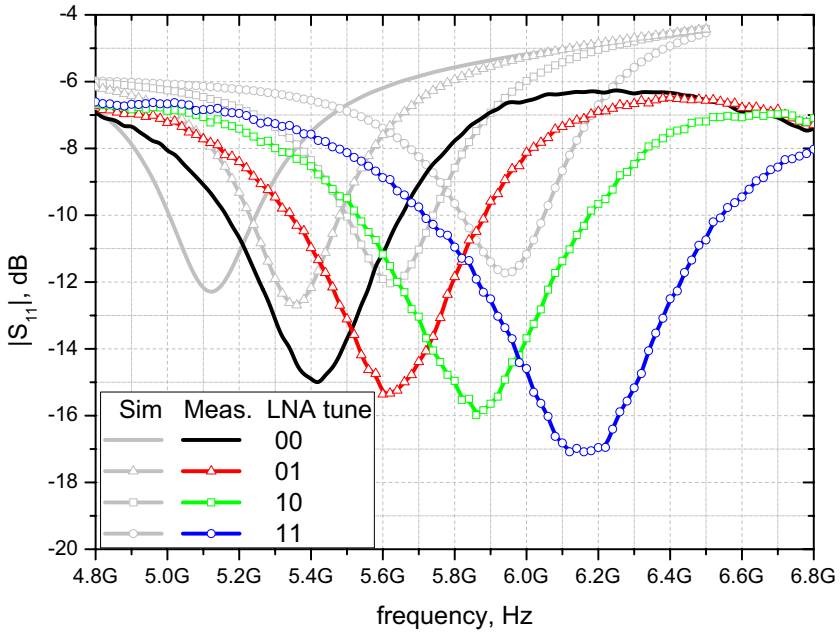


Figure 6.26: Comparison of simulated and measured insertion loss.

gain plotted in Figure 6.27 is lower by 5 dB for all gain settings if compared with simulation. This difference may be caused by lower LNA gain caused by slight mismatch at the input and by smaller gain in the following components. Analyzing Figure 6.28, we note that the measured NF is 1 dB higher than simulated for the highest achieved gain. This difference increases for smaller values of the conversion gain. It is probable, that the higher measured NF is caused in small part due to the LNA mismatch (seen when the highest conversion gain is set) and dominated by the filter noise which is not sufficiently reduced by the PGA gain. Summarizing, there is some difference between the measured and simulated performance of the receiver but it fulfills the system requirements.

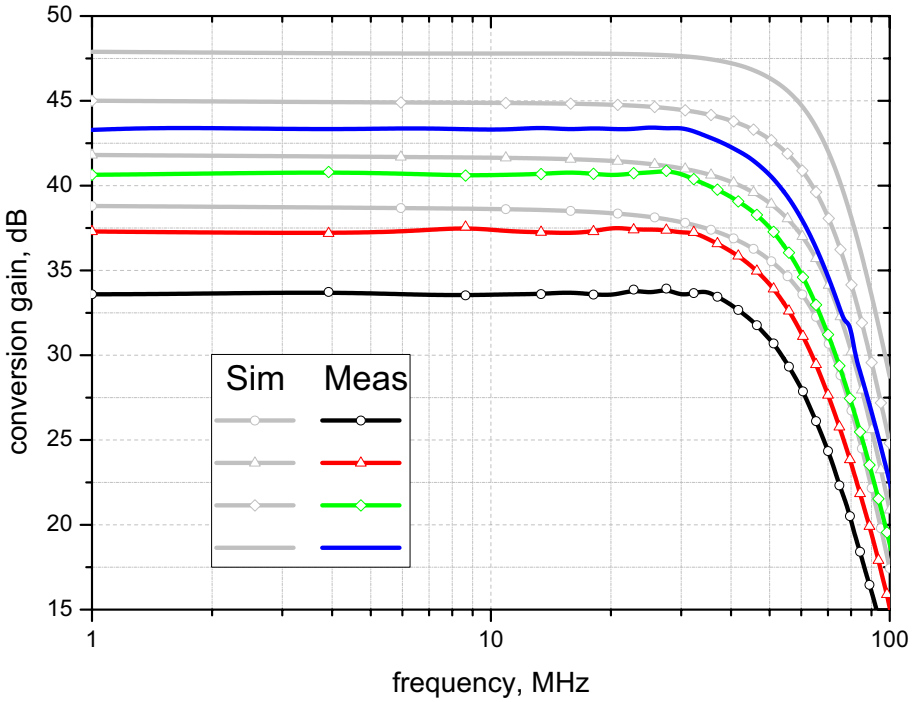


Figure 6.27: Comparison of simulated and measured conversion gain.

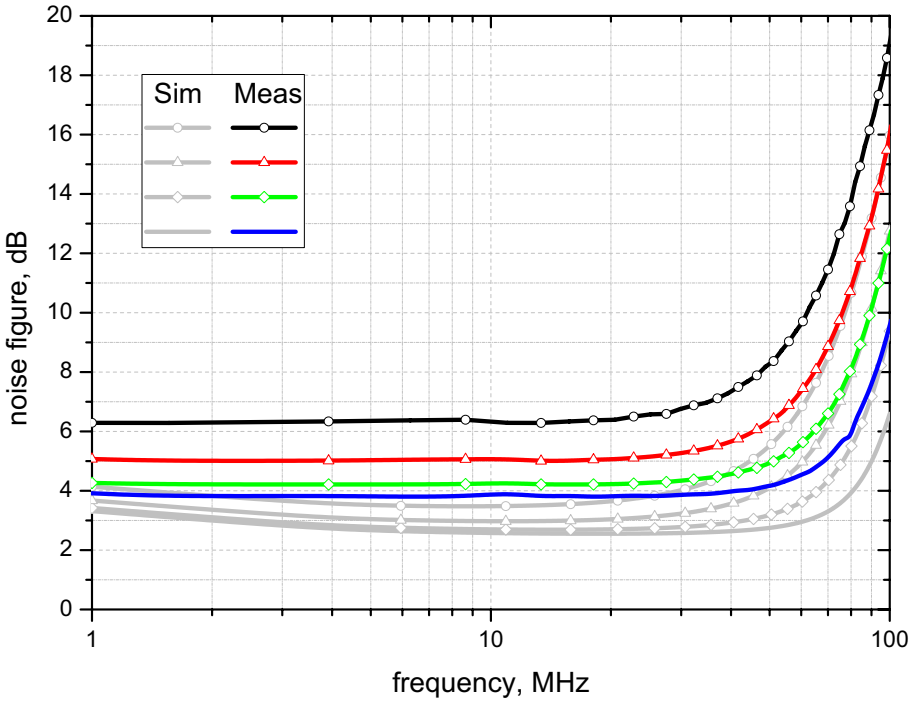


Figure 6.28: Comparison of simulated and measured noise figure.

Demonstrator Board

The demonstrator board with the characterized 5 - 6 GHz receiver was build for the WIGWAM project requirements. The board includes two rat-race hybrids, one to supply differential input RF signal to the receiver and the other to feed in the free running VCO signal to an external PLL, as shown in Figure 6.29. Additionally, two SMD variable gain amplifiers (VGA) with needed components are placed to provide high output voltage swing. This was required by other project partners who would like to perform some tests with commercial ADCs and BB processing units. The board also includes two voltage down-regulators to provide proper biasing of the receiver and the VGAs from a single 5 V supply.

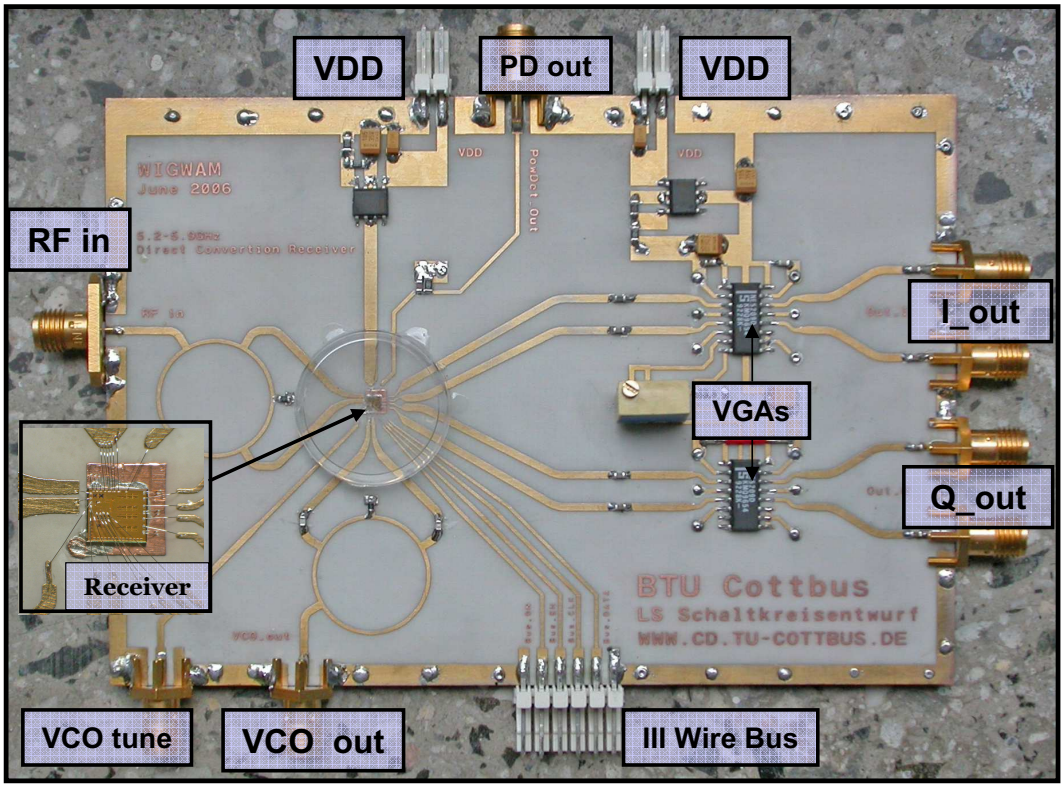


Figure 6.29: Photograph of the demonstrator board.

6.4 A Monolithically Integrated 23 - 24 GHz Tuned Down-Converter

A low loss RF board has been designed for the down-converter characterization. The dielectric material under the chip was milled away in order to level the surface of the chip with the surface of the RF board. This minimized the length of input and output bond-wires. Figure 6.30 shows a close-up of the mounted and wire-bonded down-converter chip. The chip occupies 0.9 mm x 0.9 mm of die area. Double bond-pads with two bond-wires were used for both RF inputs to minimize the bond-wire inductance. Since the down-converter has a differential structure

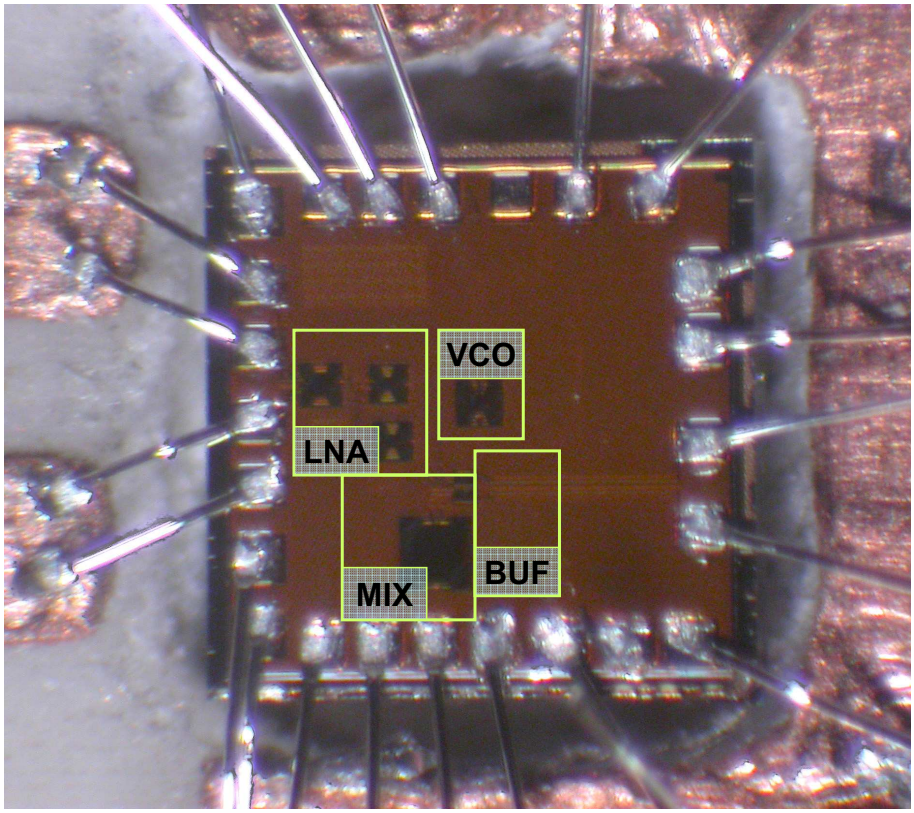


Figure 6.30: Mounted down-converter chip.

there was a need to design input and output hybrids for measurement purposes. The input hybrid employs a Wilkinson power divider where one of the branches is longer in order to provide 180°phase shift. The output hybrid operates at 5.5 GHz and employs a rat-race or circulator structure where the common mode node is terminated by 50 Ω resistance.
The photograph of the test board with the mounted receiver chip and other components is shown in Figure 6.31. A special K connector has been used to supply the input signal because of the input signal frequency range. For other

outputs standard SMA connectors were mounted. The conversion gain and noise

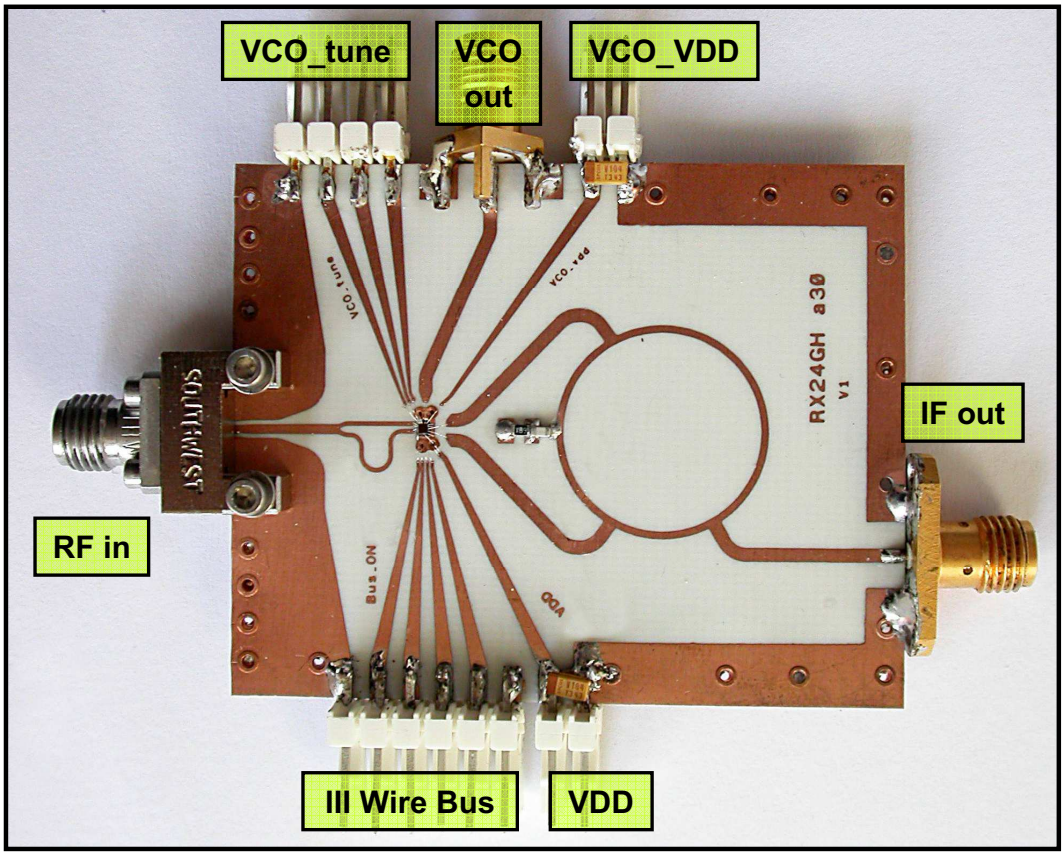


Figure 6.31: 24 GHz down-converter test board.

figure of the down-converter are shown in Figure 6.32. Depending on the LNA control signals and the VCO frequency, the proposed circuit down-converts the RF signal from 23-24 GHz to the IF of 5.5 GHz. The down-converter exhibits a conversion gain of more than 20 dB from 23 to 24 GHz. The input and output return losses are presented in Figure 6.33. The input and output of the down-converter are well matched to 50 Ω impedance. The achieved minimum input and output return losses are equal 15.2 dB and 14.1 dB, respectively. Figure 5.40 reports the measured nonlinearity of the down-converter. The measurements were performed for an input signal of 24 GHz and an IF of 5.5 GHz. The input referred 1 dB compression point is reached at P_{in} = -16.7 dBm. The measured performance of the 24 GHz down-converter is summarized in Table 6.5.

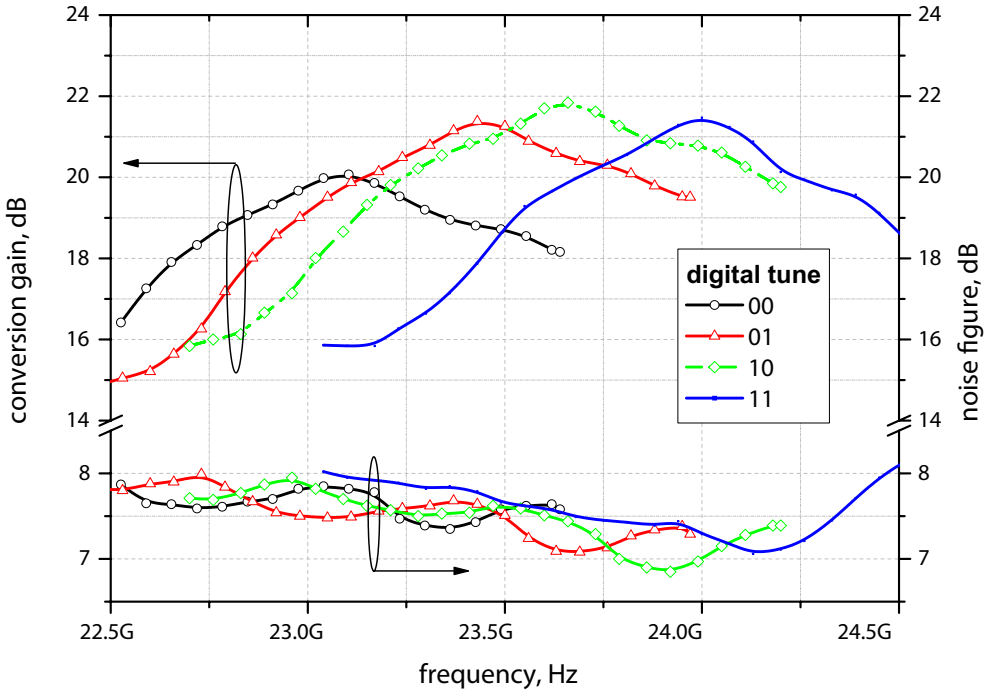


Figure 6.32: Measured conversion gain and noise figure.

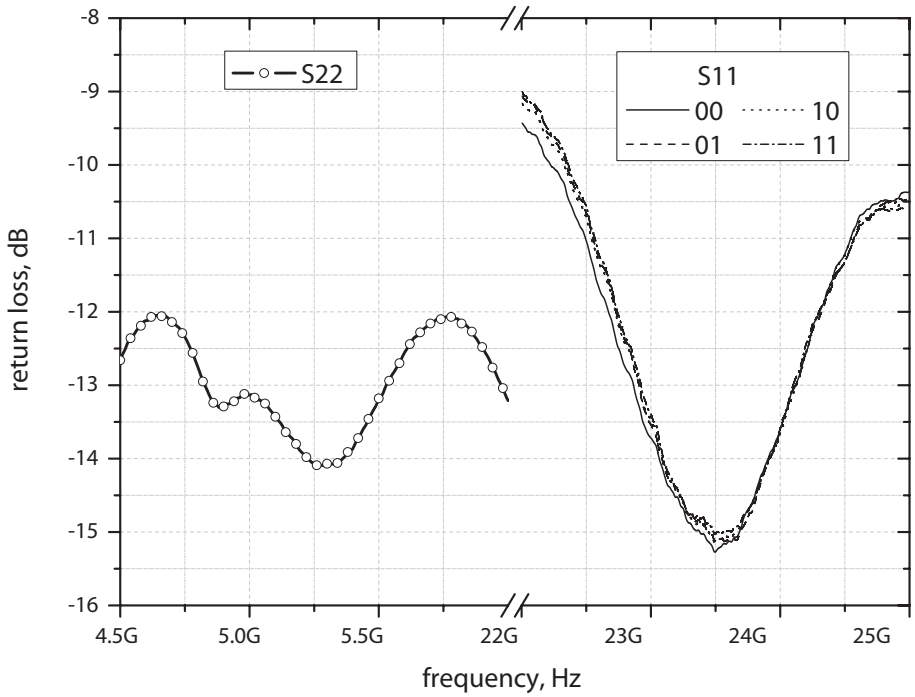


Figure 6.33: Measured input and output return loss.

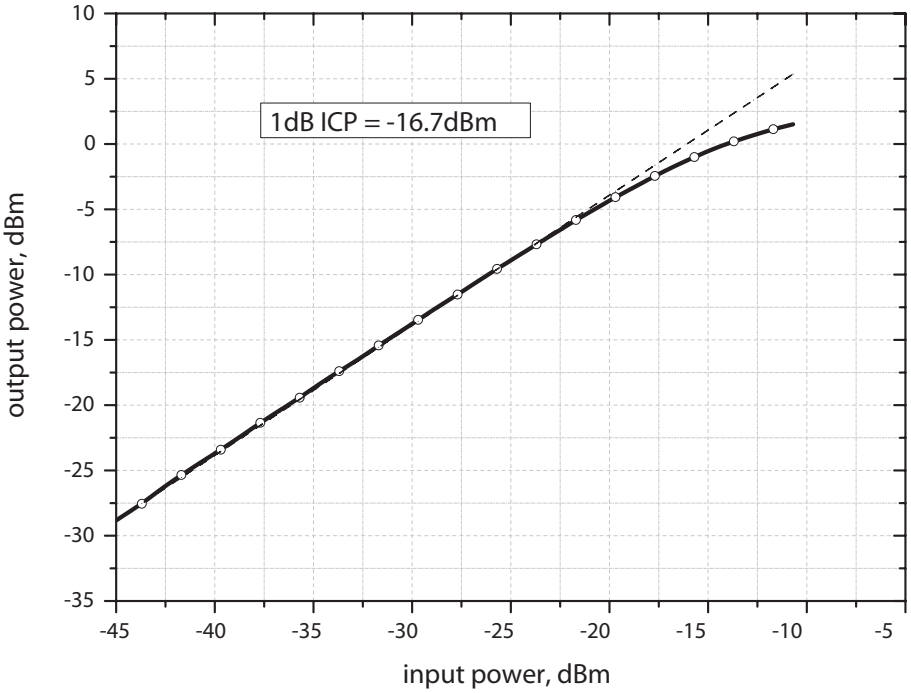


Figure 6.34: Measured input 1 dB compression point of the down-converter.

Table 6.5: Performance summary of the down-converter.

Parameter	Measurement			
Peak Gain Frequency	23.10 GHz	23.43 GHz	23.66 GHz	24.02 GHz
Peak Power Gain	20.07 dB	21.38 dB	21.84 dB	21.47 dB
Noise Figure	7.35 dB	7.08 dB	6.85 dB	7.06 dB
I/O Return Losses	< -13 dB			
1dB ICP	-16.7 dBm @ $RF_{in} = 24\,GHz$			
Power Consumption	58.5 mW @ $V_{DD} = 1.8\,V$			

Chapter 7

Conclusions and Outlook

This work reports on the development, design and implementation of a multi-band multi-standard WLAN system consisting of a 5 - 6 GHz receiver and a 24 GHz down-converter. The circuits are implemented in a standard 0.13 μm CMOS technology. The 5 - 6 GHz receiver employs a direct-conversion architecture with the tunable common-gate LNA, a quadrature demodulator and a tunable channel select filter. Additionally, the analog pre-processing loop was implemented allowing the receiver to adapt its sensitivity and linearity according to the input signal level. The receiver features a measured maximum gain of 43.4 dB and a corresponding DSB noise figure of 3.8 dB, and an input 1 dB compression point of -25.5 dBm. The circuit consumes 140 mW from a 1.5 V supply voltage. The receiver performance achieves one of the leading positions among recently reported implementations. The 24 GHz down-converter enhances the multi-band operation of the system. It down-converts the signal from the frequency range of 22.7 - 24.5 GHz to an intermediate frequency of 5.5 GHz. The circuit features a measured conversion gain of 21.5 dB, a SSB noise figure of 7 dB and an input 1 dB compression point of -17 dBm. It consumes 58.5 mW from a 1.8 V supply. The obtained results show that a standard CMOS technology is feasible for analog integrated circuits operating at frequencies higher than 20 GHz. Furthermore, the performance of the implemented down-converter is competitive with other recently reported implementations in SiGe BiCMOS technology, as shown in Table 1.2.

The next field of research would be the integration of the whole multi-band system on a single chip. Additionally, a 17 GHz receiver can be added to cover all available ISM bands, [Kienmayer 04]. Finally, a transmitter path with integrated power amplifiers ([Vasylyev 06]) could be added to fulfill an ultimate goal of the multi-band transceiver system.

Bibliography

[Abidi 95] A.A. Abidi, "Direct-conversion radio transceivers for digital communications", *in IEEE Journal of Solid-State Circuits*, pp. 1399–1410. vol.30, no.12, December 1995.

[Aparicio 02] Roberto Aparicio and Ali Hajimiri, "Capacity Limits and Matching Properties of Integrated Capacitors", *in IEEE Journal of Sold-State Circuits*, pp. 384 – 393. vol.37,no.3, March 2002.

[Bensky 00] Alan Bensky, *Short-range Wireless Communication*, Lewis Lewis & Helms LLC, 2000.

[Biggs 04] M. Biggs, A. Henley, and T. Clarkson, "Occupancy analysis of the 2.4 GHz ISM band", *in IEE Proceedings - Communications*, pp. 481 – 488. vol.151, no.5, October 2004.

[Binkley 02] D.M. Binkley, J.M. Rochelle, B.K. Swann, L.G. Clonts, and R.N. Goble, "A micropower CMOS direct-conversion, VLF receiver chip for magnetic-field wireless applications", *in IEEE Journal of Solid-State Circuits*, p. 344358. vol. 33, March 2002.

[Brandolini 05] M. Brandolini, P. Rossi, and D. Manstretta F. Svelto, "Toward multistandard mobile terminals - fully integrated receivers requirements and architectures", *in IEEE Transactions on Microwave Theory and Techniques*, pp. 1026 – 1038. issue 3, vol. 7, part 2, March 2005.

[Chandrasekha 02] V. Chandrasekhar, C.M. Hung, Y.C. Ho, and K. Mayaram, "A packaged 2.4 GHz LNA in a 0.15 um CMOS process with 2kV HBM ESD protection", *in Proceedings of the 28th European Solid-State Circuits Conference*, p. 347 350. ESSCIRC, September 2002.

[Chang 94] J. Chang, A.A. Abidi, and C.R. Viswanathan, "Flicker noise in CMOS transistors from subthreshold to strong inversion

at various temperatures", *in IEEE Transactions on Electron Devices*, pp. 1965 – 1971. issue 11, vol. 41, November 1994.

[Chang 05] Chung-Ping Chang, Cheng-Chi Yen, and Huey-Ru Chuang, "A 2.4 6GHz CMOS Broadband High-Gain Differential LNA for UWB and WLAN Receiver", *in Asian Solid-State Circuits Conference*, pp. 469 – 472, November 2005.

[Chen 03] Min Chen, K.H. Wang, Desong Zhao, Liang Dai, Z. Soe, and P. Rogers, "A CMOS Bluetooth radio transceiver using a sliding-IF architecture", *in Proceedings of the IEEE 2003 Custom Integrated Circuits Conference*, pp. 455–458, September 2003.

[Chen 05] Wei-Zen Chen, Tsorng-Lin Lee, and Tai-You Lu, "A 5-GHz direct-conversion receiver with I/Q phase and gain error calibration [WLAN applications]", *in Digest of Papers of Radio Frequency integrated Circuits (RFIC) Symposium*, pp. 201 – 204. IEEE, 12-14 June 2005.

[Crols 98] J. Crols and M.S.J. Steyaert, "Low-if topologies for high-performance analog front-ends of fully integrated receivers", *in IEEE Transactions on Circuit and Systems - II: Analog and Digital Signal processing*, pp. 1399–1410. vol.45, no.3, March 1998.

[Darabi 00] H. Darabi and A.A. Abidi, "Noise in RF-CMOS mixers: a simple physical model", *in IEEE Journal of Solid-State Circuits*, pp. 15 – 25. issue 1, vol. 35, January 2000.

[Darabi 05] H. Darabi and J. Chiu, "A noise cancellation technique in active RF-CMOS mixers", *in IEEE Journal of Solid-State Circuits*, pp. 2628 – 2632. issue 12, vol. 40, December 2005.

[Debski 07,a] W. Debski and P. Weger, "5-6 GHz Low-Power, High Linearity Differential CMOS LNA with Robust ESD Protection", *in Journal "Frequenz"*, pp. 110 – 112. 5-6/2007, vol.61, May/June 2007.

[Debski 07,b] W. Debski and P. Weger, "A Monolithically Integrated 23-24 GHz Tuned Down-Converter in 0.13 um CMOS", *in Journal "Frequenz"*, pp. 178 – 181. 7-8/2007, vol.61, July/August 2007.

[Deliyannis 99] T.L. Deliyannis, Yichuang Sun, and J.K. Fidler, *Continuous-Time Active Filter Design*, Boca Raton: CRC Press LLC, 1999.

[Eberts 05] J. Eberts, E. Grass, R. Irmer, R. Kraemer, G. Fettweis, K. Strom, G. Trankle, W. Wirnitzer, R. Witmann, H. Reumerman, E. Schulz, M. Weckerle, P. Egner, and U. Barth, "Paving the way for gigabit networking", *in IEEE Communication Magazine*, pp. 27–30. vol.43, no.4, April 2005.

[Fettweis 05] G. Fettweis, *WIGWAM: System Concept for 1 Gb/s and Beyond*, EEE 802 Plenary Meeting, Vancouver, Canada, November 2005.

[Fong 99] Keng Leong Fong and R.G. Meyer, "Monolithic RF active mixer design", *in IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, pp. 231 – 239. issue 3, vol. 46, March 1999.

[Gilbert 97] B. Gilbert, "The MICROMIXER: a highly linear variant of the Gilbert mixer using a bisymmetric Class-AB input stage", *in IEEE Journal of Solid-State Circuits*, pp. 1412 – 1423. issue 9, vol. 32, September 1997.

[Gramegna 01] G. Gramegna, M. Paparo, P.G. Erratico, and P. De Vita, "A sub-1-dB NF 2.3-kV ESD-protected 900-MHz CMOS LNA", *in IEEE Journal of Solid-State Circuits*, p. 1010 1017. issue 7, vol. 36, July 2001.

[Gresham 06] I. Gresham, Noyan Kinayman, A. Jenkins, R. Point, A. Street, Yumin Lu, Adil Khalil, R. Ito, and R. Anderson, "A fully integrated 24 GHz SiGe receiver chip in a low-cost QFN plastic package", *in Radio Frequency Integrated Circuits (RFIC) Symposium*, p. 4. IEEE, 11-13 June 2006.

[Guan 02] Xiang Guan and A. Hajimiri, "A 24GHz CMOS Front-end", *in Proceedings of the 28th European Solid-State Circuits Conference*, pp. 155 – 158. ESSCIRC 2002, September 2002.

[Guan 04,a] Xiang Guan and A. Hajimiri, "A 24-GHz CMOS front-end", *in IEEE Journal of Solid-State Circuits*, pp. 368 – 373. issue 2, vol. 39, February 2004.

[Guan 04,b] Xiang Guan, H. Hashemi, and A. Hajimiri, "A fully integrated 24-GHz eight-element phased-array receiver in silicon", *in IEEE Journal of Solid-State Circuits*, pp. 2311 – 2320. issue 12, vol. 39, December 2004.

[HFSS 07] Ansoft HFSS, *3D Electromagnetic-Field Simulator, http://www.ansoft.com*, 2007.

[Hsu 03] Cheng-Chung Hsu and Jieh-Tsorng Wu, "A highly linear 125-MHz CMOS switched-resistor programmable-gain amplifier", *in IEEE Journal of Solid-State Circuits*, pp. 1663 – 1670. issue 10, vol. 38, October 2003.

[Hyvonen 05] S. Hyvonen, K. Bhatia, and E. Rosenbaum, "An ESD-protected, 2.45/5.25-GHz dual-band CMOS LNA with series LC loads and a 0.5-V supply", *in Radio Frequency integrated Circuits (RFIC) Symposium*, pp. 43 – 46. IEEE 2005, June 2005.

[IEEE 99] IEEE, *802.11a Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications*, 1999.

[Johns 97] D.A. Johns and K. Martin, *Analog integrated circuit design*, John Wiley & Sons, New York, 1997.

[Ker 01] Ming-Dou Ker, Jeng-Jie Peng, and Hsin-Chin Jiang, "ESD test methods on integrated circuits: an overview", *in The 8th IEEE International Conference on Electronics, Circuits and Systems, 2001*, pp. 1011 – 1014. ICECS 2001, vol. 2, September 2001.

[Kienmayer 04] C. Kienmayer, R. Thüringer, M. Tiebout, W. Simbürger, and A.L. Scholtz, "An Integrated 17 GHz Front-End for ISM/WLAN Applications in 0.13 μm CMOS", *in IEEE Symposium on VLSI Circuits*, Juni 2004.

[Kivekas 01] K. Kivekas, A. Pärssinen, and K.A.I. Halonen, "Characterization of IIP2 and DC-offsets in transconductance mixers", *in IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, pp. 1028 – 1038. issue 11, vol. 48, November 2001.

[Laskar 04] J. Laskar, B. Matinpour, and S. Chakreborty, *Modern Receiver Front-Ends; Systems, Circuits, and Integration*, John Wiley & Sons, 2004.

[Leroux 02] P. Leroux, M. Steyaert, V. Vassilev, and G. Groeseneken, "A 1.3dB NF CMOS LNA for GPS with 3kV HBM ESD-protection", *in Proceedings of the 28th European Solid-State Circuits Conference*, p. 335 338. ESSCIRC, September 2002.

[Leroux 05] P. Leroux and M. Steyaert, "RF-ESD design and measurement of CMOS LNAs: a comparison between diode and inductive protection", *in Proceedings of the International Conference on Microelectronic Test Structures*, pp. 171 – 176. ICMTS 2005, April 2005.

[Li 06] Wei-Chang Li, Chao-Shiun Wang, and Chorng-Kuang Wang, "A 2.4-GHz/3.5-GHz/5-GHz Multi-Band LNA with Complementary Switched Capacitor Multi-Tap Inductor in 0.18 um CMOS", *in International Symposium on VLSI Design, Automation and Test*, pp. 1 – 4, April 2006.

[Linten 05] D. Linten, S. Thijs, M.I. Natarajan, P. Wambacq, W. Jeamsaksiri, J. Ramos, A. Mercha, S. Jenei, S. Donnay, and S. Decoutere, "A 5-GHz fully integrated ESD-protected low-noise amplifier in 90-nm RF CMOS", *in IEEE Journal of Solid-State Circuits*, pp. 1434 – 1442. issue 7, vol. 40, July 2005.

[Liu 98] William Liu and Mi-Chang Chang, "Transistor transient studies including transcapacitive current and distributive gate resistance for inverter circuits", *in IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications*, pp. 416 – 422. vol.45,no.4, April 1998.

[Liu 01] William Liu, *MOSFET models for SPICE simulation, including BSIM3v3 and BSIM4*, John Wiley & Sons, first edition, 2001.

[MacEachern 98] L.A. MacEachern and T. Manku, "A charge-injection method for Gilbert cell biasing", *in IEEE Canadian Conference on Electrical and Computer Engineering*, pp. 365 – 368. vol. 1, 24-28 May 1998.

[Maget 02] Judith Maget, *Varactors and Inductors for Integrated RF Circuits in Standard MOS Technologies*, PHD-Thesis, Universität der Bundeswehr München,Fakultät für Elektrotechnik und Informationstechnik, 2002.

[Mahdavi 02] S. Mahdavi and A.A. Abidi, "Fully Integrated 2.2-mW CMOS Front End for a 900-MHz Wireless Receiver", *in IEEE Journal of Solid-State Circuits*, pp. 662 – 669. vol. 37, May 2002.

[Momentum 07] Agilent Momentum, *3-D planar electromagnetic (EM) simulator, http://www.agilent.com*, 2007.

[Olexa 05] Ron Olexa, *Implementing 802.11, 802.16, and 802.20 Wireless Networks*, Elsevier Inc., 2005.

[Park 98] Min Park, Seonghearn Lee, Cheon Soo Kim, Hyun Kyu Yu, and Kee Soo Nam, "The detailed analysis of high Q CMOS-compatible microwave spiral inductors in silicon technology",

in IEEE Transactions on Electron Devices, pp. 1953 – 1959. issue 9, vol. 45, September 1998.

[Razavi 98] Behzad Razavi, *RF microelectronics*, Prentice Hall, first edition, 1998.

[Rijns 96] J.J.F. Rijns, "CMOS low-distortion high-frequency variable-gain amplifier", *in IEEE Journal of Solid-State Circuits*, pp. 1029 – 1034. issue 7, vol. 31, July 1996.

[Rofougaran 96] A. Rofougaran, J.Y.-C. Chang, and M. Rofougaran A.A. Abidi, "A 1 GHz CMOS RF front-end IC for a direct-conversion wireless receiver", *in IEEE Journal of Solid-State Circuits*, pp. 880 – 889. issue 7, vol. 31, July 1996.

[Ryynanen 01] J. Ryynanen, K. Kivekas, J. Jussila, A. Parssinen, and K.A.I. Halonen, "A dual-band RF front-end for WCDMA and GSM applications", *in IEEE Journal of Solid-State Circuits*, pp. 1198 – 1204. issue 8, vol. 36, August 2001.

[Salerno 05] R. Salerno, M. Tiebout, H. Paule, M. Streibl, C. Sandner, and K. Kropf, "ESD-protected CMOS 3-5 GHz wideband LNA+PGA design for UWB", *in Proceedings of the 31st Solid-State Circuits Conference*, pp. 219 – 222. ESSCIRC 2005, September 2005.

[Samavati 00] H. Samavati, H.R. Rategh, and T.H. Lee, "A 5-GHz CMOS wireless LAN receiver front end", *in IEEE Journal of Solid-State Circuits*, pp. 765 – 772. issue 5, vol. 35, May 2000.

[Sansen 99] W. Sansen, "Distortion in elementary transistor circuits", *in IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, pp. 315 – 325. vol. 46, March 1999.

[Shaeffer 97] D.K. Shaeffer and T.H. Lee, "A 1.5 V 1.5 GHz CMOS low noise amplifier", *in IEEE Journal of Solid-State Circuits*, pp. 745 – 759. vol.32, no.5, May 1997.

[Sivonen 05] P. Sivonen, A. Vilander, and A. Pärssinen, "Cancellation of second-order intermodulation distortion and enhancement of IIP2 in common-source and common-emitter RF transconductors", *in IEEE Transactions on Circuits and Systems-I:Regular Papers*, pp. 305 – 317. vol. 52, February 2005.

[Sonmez 05] E. Sonmez, S. Chartier, C. Schick, A. Trasser, and H. Schumacher, "Fully integrated differential 24 GHz receiver using a 0.8 um SiGe HBT technology", *in European Microwave Conference*, p. 4. vol. 2, 4-6 October 2005.

[Tang 04] Siu-Kei Tang, Cheong-Fat Chan, Chiu-Sing Choy, and Kong-Pang Pun, "CMOS RF LNA with high ESD immunity", *in Proceedings of the 2004 IEEE Asia-Pacific Conference on Circuits and Systems*, p. 321324. vol. 1, December 2004.

[Terrovitis 99] M.T. Terrovitis and R.G. Meyer, "Noise in current-commutating CMOS mixers", *in IEEE Journal of Solid-State Circuits*, pp. 772 – 783. issue 6, vol. 34, June 1999.

[Treankle 01] G. Treankle, *Multiplizierungchaltung*, Deutsches Patentamt mit der Aktenzahl DE 101 34 754 A1, 2001.

[Vasylyev 06] Andriy Vasylyev, *Integrated RF Power Amplifier Design in Silicon-Based Technologies*, PHD-Thesis, Brandenburgische Technische Universität Cottbus,Fakultät für Mathematik, Naturwissenschaften und Informatik, 2006.

[Wang 05] A.Z.H. Wang, Haigang Feng, Rouying Zhan, Haolu Xie, Guang Chen, Qiong Wu, X. Guan, Zhihua Wang, and Chun Zhang, "A review on RF ESD protection design", *in IEEE Transactions on Electron Devices*, pp. 1304 – 1311. issue 7, vol. 52, July 2005.

[Ytterdal 03] Trond Ytterdal, Yuhua Cheng, and Tor Fjeldly, *Device modeling for analog and RF CMOS circuit design*, John Wiley & Sons, first edition, 2003.

[Zhou 06] Yijun Zhou, Chee Piew Yoong, Leong Siew Weng, Yin Jee Khoi, M. Chia Yan Wah, K. Ang Chai Moy, and D. Wee Tue Fatt, "A 5 GHz dual-mode WiMAX/WLAN direct-conversion receiver", *in IEEE International Symposium on Circuits and Systems*, p. 4. ISCAS, 21-24 May 2006.

[Zito 06] D. Zito, B. Neri, and R. Massini, "54 dB Image Rejection Fully Integrated Receiver for Multi-standard 5-GHz WLANs", *in The 1st European Microwave Integrated Circuits Conference*, pp. 187 – 189. IEEE, September 2006.